

BIIS 1200
Compatible

iCOM[®]

**SERVICE
MANUAL**

UHF FM TRANSCEIVER

IC-F2610

Icom Inc.

INTRODUCTION

This service manual describes the latest service information for the **IC-F2610** UHF FM TRANSCEIVER at the time of publication.

To upgrade quality, any electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

DANGER

NEVER connect the transceiver to an AC outlet or to a DC power supply that uses more than 16 V. This will ruin the transceiver.

DO NOT expose the transceiver to rain, snow or any liquids. **DO NOT** reverse the polarities of the power supply when connecting the transceiver.

DO NOT apply an RF signal of more than 20 dBm (100 mW) to the antenna connector. This could damage the transceiver's front end.

MODEL	VERSION	FREQ.RANGE (MHz)	TX PWR (W)	CH. SPACING (kHz)	UNIT ^{*1}	SPEAKER ^{*1}	MEMORY ^{*1}
IC-F2610	EUR-8	400-430	25/10/2	25/12.5	None	None	None
	EUR-9	440-490					
	EUR-10	490-520					
	EUR-11	440-490	10/5/2				
	EUR-12	400-430	25/10/2				
	EUR-13	440-490	10/5/2				
	EUR-14						
	EUR-01	400-430	25/10/2		None	None	
	EUR-02	440-490					
	EUR-71	400-430			UT-103 ^{*3}	SP-22	EX-1761
EUR-72	440-490						

*1: Accessories

*2: Same as that supplied with the [5-tone] version

*3: Same as that supplied with the [BIIS] version



ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

<SAMPLE ORDER>

1110003571 S.IC MC3372SVM IC-F2610 MAIN UNIT 5 pieces
8810009370 Screw PH BT M3x12 ZK IC-F2610 Bottom cover 10 pieces

Addresses are provided on the inside back cover for your convenience.

REPAIR NOTES

1. Make sure a problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated tuning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 40 dB to 50 dB attenuator between the transceiver and a deviation meter or spectrum analyzer when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.

EXPLICIT DEFINITIONS

FREQUENCY COVERAGE

Lo-band	400–430 MHz
Middle-band	440–490 MHz
Hi-band	490–520 MHz

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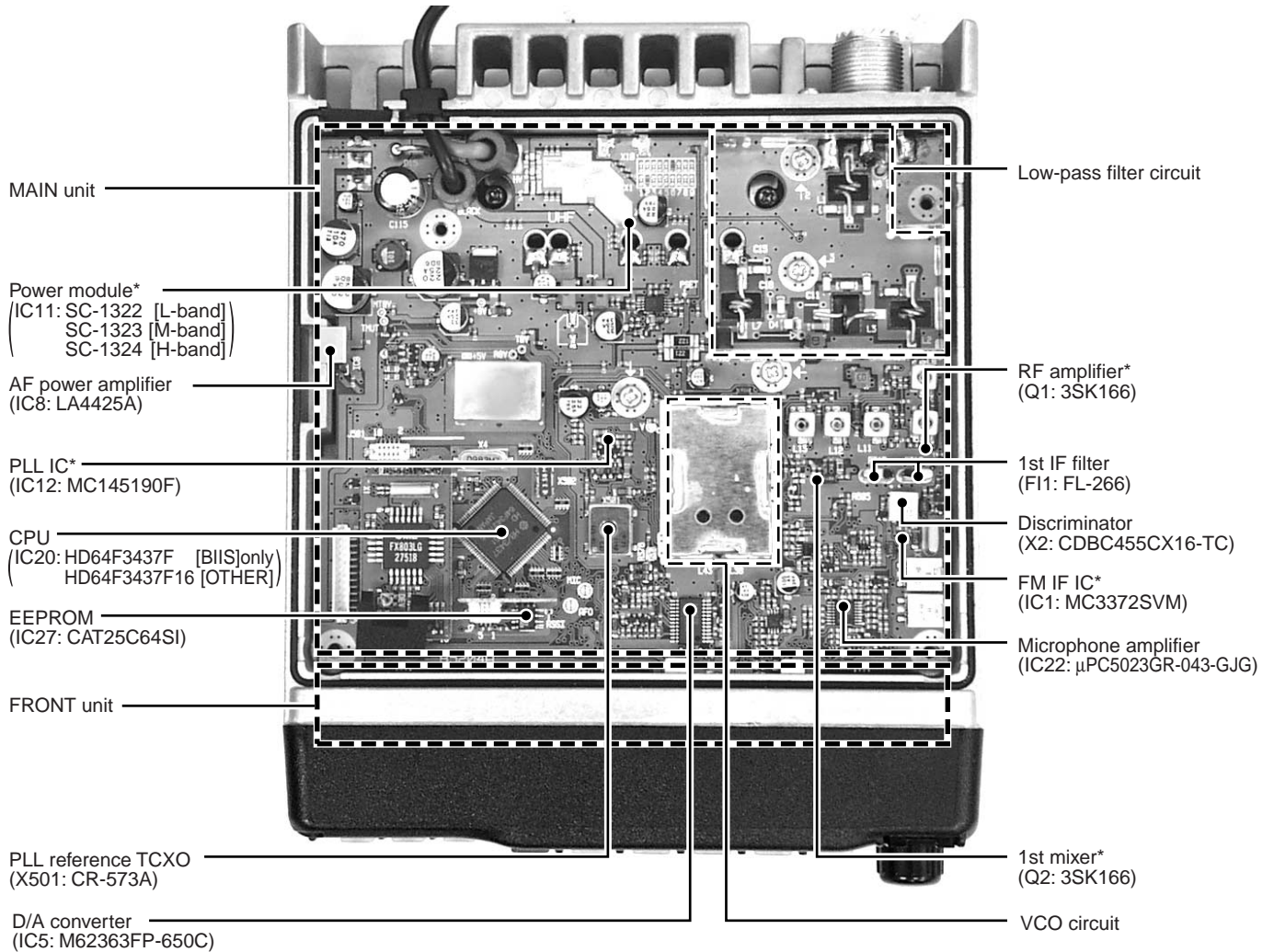
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SECTION 1 SPECIFICATIONS

GENERAL	Measurement method	ETS 300 086		
	Frequency coverage	400–430 MHz [L-band], 440–490 MHz [M-band], 490–520 MHz [H-band]		
	Number of channels	128 (16 ch × 8 banks)		
	Type of emission	16K0F3E (25 kHz; [Wide]) 8K50F3E (12.5 kHz; [Narrow])		
	Operating temperature range	–20°C to +55°C		
	Power supply voltage	13.2 V DC (negative ground)		
	Current drain (approx.)	TX	max. power	8.0 A [25 W], 6.5 A [10 W]
			max. audio	1.2 A
		RX	stand-by	700 mA
	Antenna connector	SO-239 (50 Ω)		
	Dimensions (proj. not included)	150(W) × 50(H) × 180(D) mm		
Weight	1.5 kg			
TRANSMITTER	Output power	25 W/10 W/2.5 W [25 W] type, 10 W/5 W/2.5 W [10 W] type		
	Modulation system	Variable reactance frequency modulation		
	Max. frequency deviation	±5.0 kHz [Wide] ±2.5 kHz [Narrow]		
	Frequency error	±1.5 kHz		
	Spurious emissions	0.25 μW (≤ 1 GHz), 1.00 μV (> 1 GHz)		
	Adjacent channel power	70 dB [Wide] 60 dB [Narrow]		
	Audio frequency response	+2 dB to –5 dB of 6 dB/octave range from 300 Hz to 3000 Hz [Wide]/from 300 Hz to 2550 Hz [Narrow]		
	Audio harmonic distortion	5 % (40 % Dev.)		
	Residual modulation (with CCITT filter)	45 dB minimum: 55 dB typical [Wide] 40 dB minimum: 50 dB typical [Narrow]		
	Limiting	70–100 % of modulation		
	Microphone connector	8-pin modular (600 Ω)		
	RECEIVER	Intermediate frequency	1st: 30.875 MHz 2nd: 455 kHz	
Sensitivity		–2 dBμV emf (at 20 dB SINAD)		
Squelch sensitivity		–4 dBμV emf (Threshold)		
Adjacent channel selectivity		70 dB [Wide] 60 dB [Narrow]		
Spurious response		70 dB		
Intermodulation		70 dB typical		
Audio frequency response		+2 dB to –5 dB of 6 dB/octave range from 300 Hz to 3000 Hz [Wide]/from 300 Hz to 2550 Hz [Narrow]		
Hum and noise (with CCITT filter)		45 dB minimum: 55 dB typical [Wide] 40 dB minimum: 50 dB typical [Narrow]		
Audio output power		3.5 W at 10% distortion with a 4 Ω load		
External SP connector		2-conductor 3.5 (d) mm (1/8")/4 Ω		

All stated specifications are subject to change without notice or obligation.

SECTION 2 INSIDE VIEW

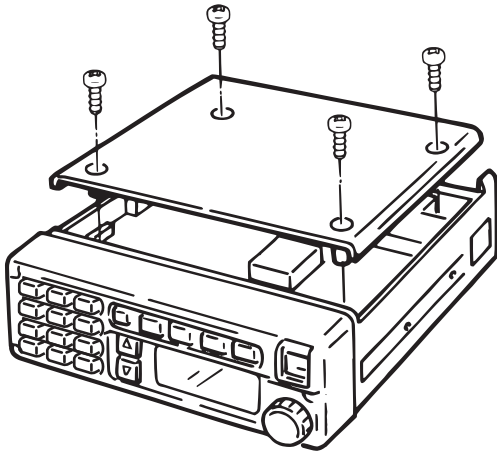


*Located under side of the point

SECTION 3 DISASSEMBLY AND OPTION INSTRUCTIONS

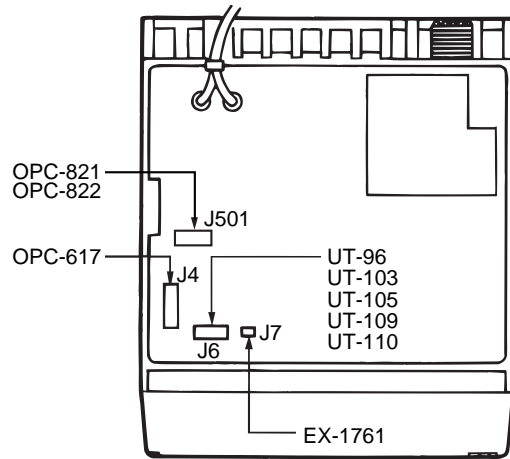
• Opening cover

Remove 4 screws from bottom cover.

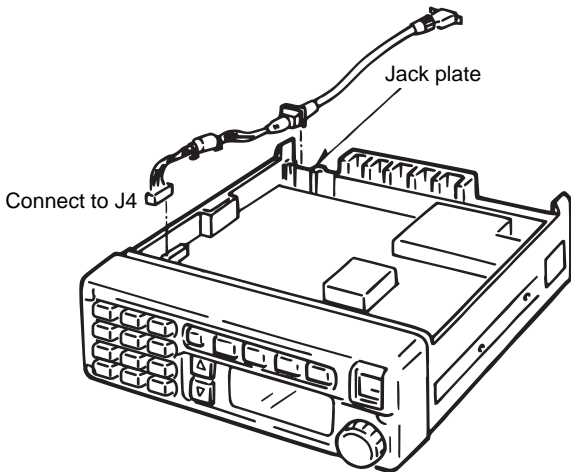


• Installation location

- OPC-617 ACC CABLE
- OPC-821 AVL CONNECT CABLE
- OPC-822 INTERFACE CABLE
- UT-96 5-TONE UNIT
- UT-103 FFSK Logic Board
- UT-105 SmarTrunk II™ Logic Board
- UT-109 VOICE SCRAMBLER UNIT (Non-rolling type)
- UT-110 VOICE SCRAMBLER UNIT (Rolling type)
- EX-1761 MEMORY EXPANSION UNIT

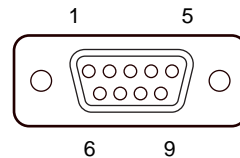


• OPC-617 connection



Break the jack plate using cutting pliers to connect the OPC-617.

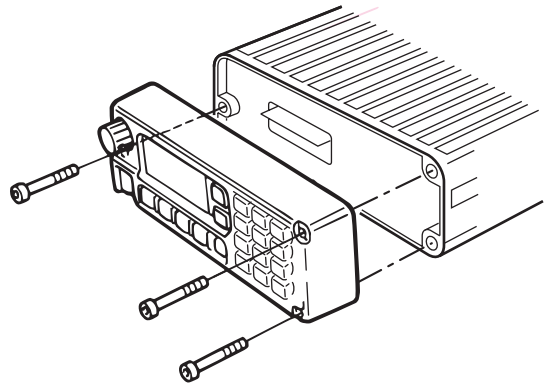
PIN ASSIGNMENT



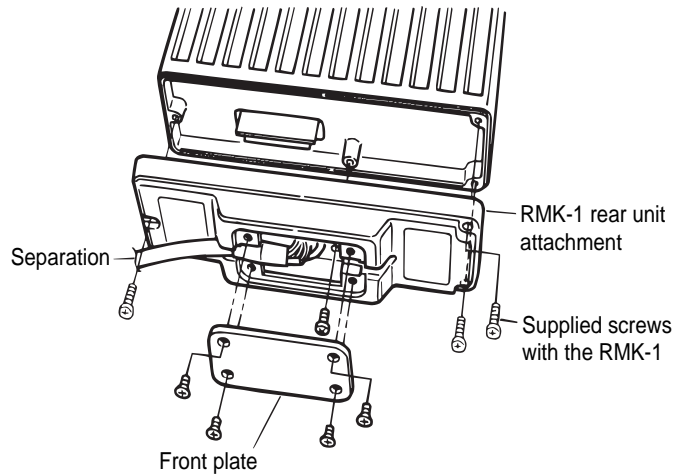
Pin No.	Terminal name	Description	Specification
1	DIM	Backlight control input	+5 to +30 V for dark
2	PAAF	AF output for public address and Ext SP functions	0 to 330 mV rms/ 47 kΩ
3	DISC	AF output for a terminal unit	330 mV rms/100 kΩ
4	IN	AF input for a terminal unit	330 mV rms/1200 bps
5	PTT	PTT control input	0 V for transmit
6	HORN	Grounded when receiving the specified call	Less than 50 mA when grounded
7	PAAF ⊖	Ground for PAAF	—
8	DISC ⊖	Ground for terminal output	—
9	IN ⊖	Ground for terminal input	—

• **RMK-1 connection**

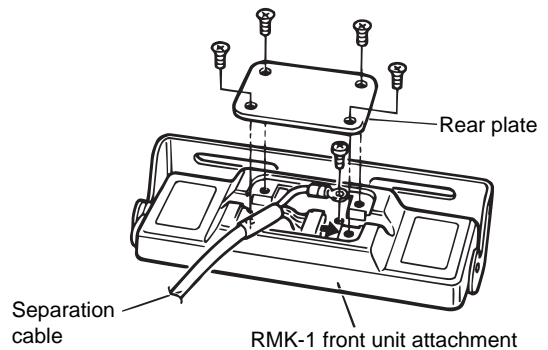
- ① Remove 3 allen-socket bolts from the front plate using an allen-wrench (1/32 in).
- ② Separate the front unit from the transceiver main unit.



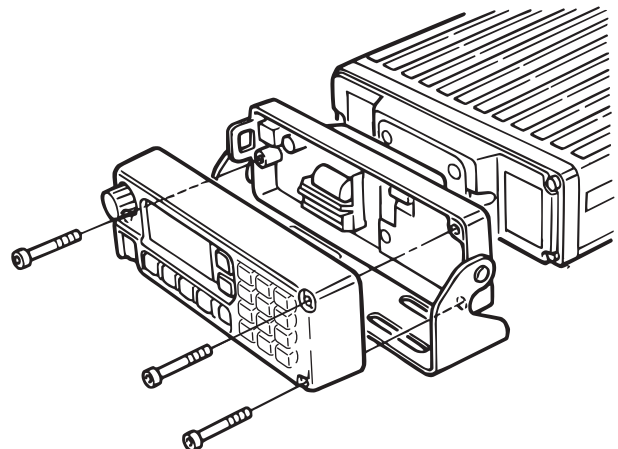
- ③ Attach the 'RMK-1 rear unit attachment' to the transceiver main unit using the supplied screws.
- ④ Remove 4 screws from the attachment to open the front plate.
- ⑤ Connect an optional separation cable OPC-609 (1.9 m) to the inside of the front plate and tighten the cable lug using the screw.
- ⑥ Re-attach the front plate.



- ⑦ Remove 4 screws from the 'RMK-1 front unit attachment' to open the rear plate.
- ⑧ Connect the other end of the optional separation cable to the attachment and tighten the cable lug using the screw.
- ⑨ Re-attach the rear plate.



- ⑩ Attach the front unit and attachment with the 3 removed allen-socket bolts.



SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT (MAIN UNIT)

The antenna switching circuit functions as a low-pass filter while receiving and a resonator circuit while transmitting. The circuit does not allow transmit signals to enter receiver circuits.

Received signals enter the antenna connector (J1) and pass through the low-pass filters (L1–L3, C2, C3, C8–C10, C415). The filtered signals are passed through the $\lambda/4$ type antenna switching circuit (D5, D6, L5) and then applied to the RF circuit.

4-1-2 RF CIRCUIT (MAIN UNIT)

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit pass through the two-stage tunable bandpass filters (D7, D8, L8, L9). The filtered signals are amplified at the RF amplifier (Q1) and then enter the another three-stage tunable bandpass filters (D9–D11, D514, L12, L13, L507) to suppress unwanted signals. The filtered signals are applied to the 1st mixer circuit.

D7–D11 and D514 employ varactor diodes, that are controlled by the PLL lock voltage, to track the bandpass filter. These varactor diodes tune the center frequency of an RF pass band for wide bandwidth receiving and good image response rejection.

4-1-3 1ST MIXER AND 1ST IF CIRCUITS (MAIN UNIT)

The 1st mixer circuit converts the received signal to fixed frequency of the 1st IF signal with the PLL output frequency. By changing the PLL frequency, only desired frequency will pass through a pair of crystal filters at the next stage of the 1st mixer.

The RF signals from the bandpass filter are mixed with the 1st LO signals, which come from the Rx VCO circuit via the LO amplifier (Q3), at the 1st mixer circuit (Q2) to produce a 30.875 MHz 1st IF signal. The 1st IF signal is passed through the matching circuit (L14, L15) and a pair of crystal filters (F11a/b) in order to obtain selection capability and to pass only the desired signals. The filtered signal is applied to the 2nd IF circuit after being amplified at the 1st IF amplifier (Q4).

4-1-4 2ND IF AND DEMODULATOR CIRCUITS (MAIN UNIT)

The 2nd mixer circuit converts the 1st IF signal into a 2nd IF signal. The double-conversion superheterodyne system (which convert receive signals twice) improves the image rejection ratio and obtains stable receiver gain.

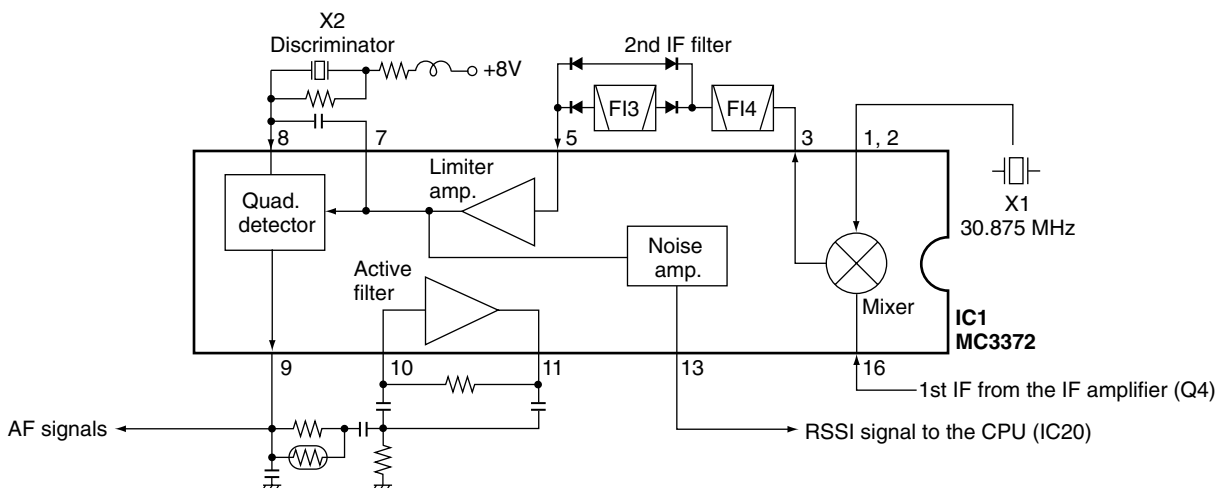
The 1st IF signal from the IF amplifier (Q4) is applied to the 2nd mixer section of the FM IF IC (IC1, pin 16) and is then mixed with the 2nd LO signal for conversion into 455 kHz 2nd IF signal.

IC1 contains the 2nd mixer, 2nd local oscillator, limiter amplifier, quadrature detector, active filter and noise amplifier circuit. The local oscillator section and X1 generates the 30.420 MHz 2nd LO signal.

The 2nd IF signal from the 2nd mixer (IC1, pin 3) passes through the ceramic filters (F13 and F14) during narrow channel spacing selection or passes through F14 (bypassing F13) only during wide channel spacing selection to suppress unwanted heterodyne frequencies signals via the N/W switches (D501, D502).

The filtered signal is applied to the quadrature detector section in the FM IF IC to demodulate the 2nd IF signal into AF signals using the ceramic discriminator (X2) after being amplified at the limiter amplifier section (pin 5). The demodulated AF signals are output from pin 9 of the IC and applied to the AF circuit via the receiver mute circuit.

• 2ND IF AND DEMODULATOR CIRCUITS



The N/W switches (D501, D502) select a ceramic filter (F13 or bypass), and the other N/W switch (Q61) adjusts the input level of the FM IF IC (IC1, pin 8) to switch the bandwidth depending on the NWC signal from the CPU (IC20, pin 57). When NWC signal becomes high level, bandwidth setting is wide.

4-1-5 AF AMPLIFIER CIRCUIT (MAIN UNIT)

The AF amplifier circuit amplifies the demodulated AF signals to drive a speaker.

The AF signals from the FM IF IC (IC1, pin 9) are amplified at the AF amplifier (IC2), and are then applied to the high-pass filter circuit (IC3a/b). The high-pass filter characteristics are controlled by the HFSW signal from the CPU (IC20, pin 60). When HFSW signal becomes high level, the cut-off frequency is shifted higher to remove CTCSS or DTCS signals.

The filtered AF signals from the high-pass filter (IC3, pin 1) are passed through the de-emphasis circuit (R68, C74) with frequency characteristics of -6 dB/octave, and are then applied to the electronic volume controller (IC7, pin 2) via the AF mute switch (Q6).

The output AF signals from the electronic volume controller (IC7, pin 9) are applied to the AF power amplifier (IC8) to drive the speaker.

4-1-6 RECEIVE MUTE CIRCUITS (MAIN UNIT)

• NOISE SQUELCH

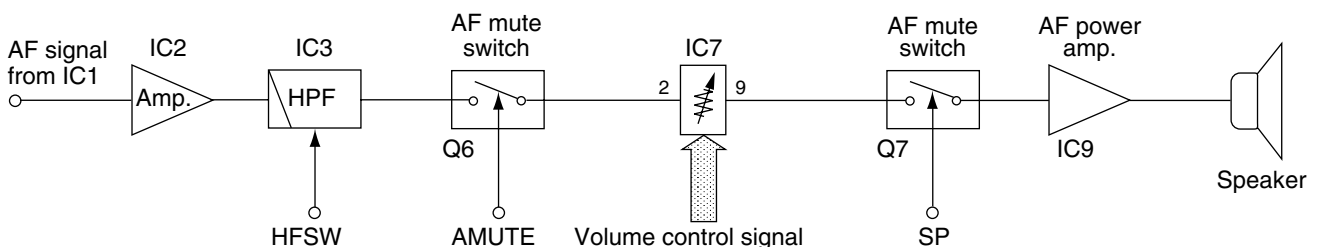
A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

Some noise components in the AF signals from the FM IF IC (IC1, pin 9) are passed through the active filter section in the IC (pins 10, 11). The N/W switch (Q62) adjusts the input noise level to the IC between wide and narrow bandwidth. When NWC signal which is applied to Q62 becomes high level, bandwidth setting is wide.

The noise signals from the FM IF IC (IC1, pin 11) are passed through the level controller (IC5, pins 21, 22) and are then converted into the pulse-type signals (NOIS) at the noise detector circuit (Q9, Q10).

The NOIS signal from the noise detector (Q10) is applied to the CPU (IC20, pin 32). The CPU then analyzes the noise condition and controls the AMUT (pin 56) and SP (pin 79) ports to toggle the AF mute switches (Q6, Q7).

• AF CIRCUIT



• CTCSS AND DTCS

The tone squelch circuit detects AF signals and opens the squelch only when receiving a signal containing a matching subaudible tone (CTCSS or DTCS). When tone squelch is in use, and a signal with a mismatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

A portion of the AF signals from the AF amplifier (IC2) pass through the low-pass filter (Q503) and are then applied to the CTCSS decoder inside the CPU (IC20, pin 43) via the CDEC line to control the AMUT and SP ports.

4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT (FRONT AND MAIN UNITS)

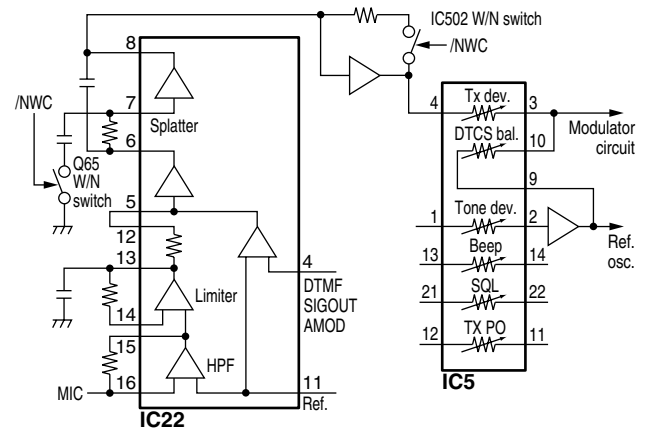
The microphone amplifier circuit amplifies audio signals from the microphone, within $+6$ dB/octave pre-emphasis characteristics, to a level needed for the modulation circuit.

AF signals (MIC) from the FRONT unit via J5 (pin 10) are applied to the audio switch (IC25). While transmitting, the MCON signal from the CPU is high and the AF signals is passed through IC25 to the microphone amplifier circuit.

The AF signals from IC25 are applied to the microphone amplifier (IC22) via the pre-amplifier (IC21b). The amplified signals are applied to the limiter amplifier in IC22.

The entered signals are pre-emphasized with $+6$ dB/octave at a limiter amplifier, then passed through a splatter filter section in IC22. The output signals from pin 8 pass through the level controller (IC5, pins 4, 3) via the buffer amplifier (IC503), and are then applied to the modulation circuit (D46).

• MICROPHONE AMPLIFIER CIRCUIT



The N/W switches (IC502, Q65) are connected to the input lines of the splatter filter section (IC22) and buffer amplifier (IC503) respectively. The N/W switches (IC502, Q65) are controlled by the /NWC signal from Q505 to adjust filter cut-off frequency (by Q65) and maximum frequency deviation (by IC502).

4-2-2 MODULATION CIRCUIT (MAIN UNIT)

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone AF signals.

The AF signals from the level controller (IC5) change the reactance of varactor diode (D46) to modulate the oscillated signal at the Tx VCO circuit (Q23). The modulated VCO signal is amplified at the buffer amplifiers (Q19, Q20) and is then applied to the drive amplifier circuit via the T/R switch (D17).

The CTCSS/DTCS signals from the CPU (IC20, pin 44) are amplified at the buffer amplifier (Q504). The amplified signals pass through the level controller (IC5, pins 1, 2) and are then applied to VCO circuit via the low-pass filter (IC21a).

When /NWC signal which is applied to the N/W switch (Q64) becomes high level, the N/W switch (Q64) changes the input level of the level controller (IC5), thus narrowing the bandwidth.

4-2-3 DRIVE/POWER AMPLIFIER CIRCUITS (MAIN UNIT)

The amplifier circuit amplifies the VCO oscillating signal to an output power level.

The signal from the buffer amplifier (Q20) passes through the T/R switch (D17), and is amplified at the drive amplifiers (Q17–Q15) and power module (IC11) to obtain 10 W or 25 W (depending on versions) of RF power.

The amplified signal is passed through the antenna switching circuit (D4), low-pass filter and APC detector. Then the signal is applied to the antenna connector.

The collector voltages for driver (Q16) come from the MT8V regulator (Q38, D28). The transmit mute switch (Q39) controls the MT8V regulator when transmit mute is necessary.

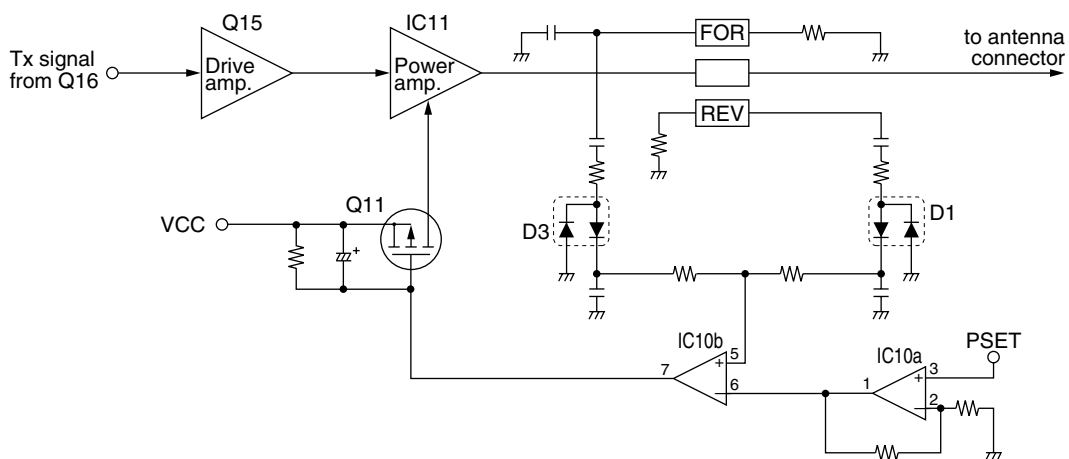
4-2-4 APC CIRCUIT (MAIN UNIT)

The APC circuit protects the power module (IC11) from a mismatched output load and stabilizes the output power.

The APC detector circuit detects forward signals and reflection signals at D3 and D1 respectively. The combined voltage is at a minimum level when the antenna impedance is matched at 50 Ω and is increased when it is mismatched.

The detected voltage is applied to the inverse amplifier (IC10b, pin 5), and the power setting voltage (PSET) is applied to the other input (IC10b, pin 6) via the amplifier (IC10a). When antenna impedance is mismatched, the detected voltage exceeds the power setting voltage. Then the output voltage of the inverse amplifier (IC10b, pin 7) controls the input current of the power module (IC11) to reduce the output power via the APC driver (Q11).

• APC CIRCUIT



4-3 PLL CIRCUITS

4-3-1 PLL CIRCUIT (MAIN UNIT)

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL circuit consists of the PLL IC, charge pump, loop filter and reference oscillator and employs a pulse swallow counter.

Oscillated signals from the VCO via the buffer amplifiers (Q19, Q18) are prescaled in the PLL IC (IC12, pin 11) based on the divided ratio (N-data). The PLL IC detects the out-of-step phase using the reference frequency and outputs it from pin 6 (IC12). The output signal is passed through the charge pump (Q30–Q33) and loop filters (R154/C181, R153/C179), and is then applied to the VCO circuit as the lock voltage.

The accelerator switch (IC13) selects the effective loop filter to accelerate the PLL lock up speed.

The lock voltage is also used for the receiver tunable band-pass filters to match the filter's center frequency to the desired receive frequency. The lock voltage is amplified at the buffer amplifier (Q29) and is then applied to the band-pass filters (D7–D11, D514) as center frequency control signal.

4-3-2 VCO CIRCUIT (MAIN UNIT)

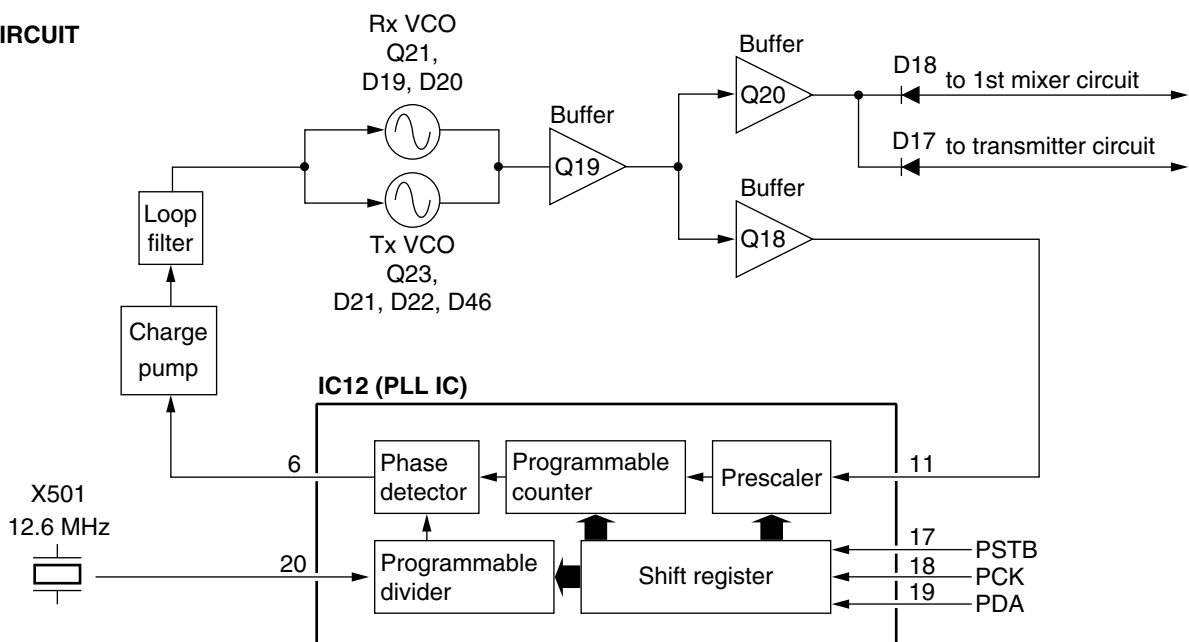
The VCO circuit contains a separate Rx VCO (Q21, D19, D20) and Tx VCO (Q23, D21, D22, D46). The oscillated signal is amplified at the buffer amplifiers (Q19, Q20) and is then applied to the T/R switches (D17, D18). Then the receive 1st LO (Rx) signal is applied to the 1st mixer (Q2) via the LO amplifier (Q3) and the transmit (Tx) signal to the driver (Q17).

A portion of the signal from the buffer amplifier (Q19) is fed back to the PLL IC (IC12, pin 11) via the another buffer amplifier (Q18) as the comparison signal.

4-4 POWER SUPPLY CIRCUIT VOLTAGE LINE

LINE	DESCRIPTION
HV	The voltage from the external power connector.
VCC	Same voltage as the HV line passed through the power control circuit (Q12, Q14) controlled by PWON signal from the CPU (IC20, pin 77).
CPU5V	Common 5 V converted from the HV line at the 5V regulator circuit (IC17). This voltage is supplied to the CPU regardless of the power switch.
+5V	Common 5 V converted from the VCC line at the +5V regulator circuit (Q42, Q43, D30) using the CPU5V line voltage as the reference.
+8V	Common 8 V converted from the VCC line at the +8V regulator circuit (IC16).
R8V	Receive 8 V converted from the VCC line at the R8V regulator circuit (Q36, Q37, D27) using the +8V line voltage as the reference and controlled by VRX signal from the CPU (IC20, pin 76).
T8V	Transmit 8 V converted from the VCC line at the T8V regulator circuit (Q40, Q41, D29) using the +8V line voltage as the reference and controlled by VTX signal from the the CPU (IC20, pin 75).
MT8V	Transmit 8 V converted from the VCC line at the MT8V regulator circuit (Q38, D28) using the +8V line voltage as the reference and controlled by TMUT signal from the the CPU (IC20, pin 62).
FVPP	Common 12 V converted from the +12V regulator circuit (IC506, Q508, Q509) using the VCC line. The circuit is controlled by the FVPC line from the CPU (IC20, pin 10).
+18V	Common 18 V converted from the +18V DC/DC convertor circuit (IC18, Q44, D31–D33) using the +8V line. The output voltage is applied to the buffer amplifier (Q29) and loop filter (IC13, Q30–Q33).

• PLL CIRCUIT



4-5 UT-103 CIRCUIT DESCRIPTION

4-5-1 GENERAL

IC1 is the FFSK modem IC which is controlled by serial data bus line ("CCS", "SI", "SO", "SCK", "CIRQ" signals) from the IC-F1610's CPU. The IC is composed FFSK transmitting and receiving circuit, data register circuits, transmitting and receiving data buffer circuits, and so on.

X1 is oscillated 4.032 MHz reference signal to the IC1.

4-5-2 DECODEING CIRCUIT

The input signal from the J1, pin 23 (IC-F1610's MAIN unit) via the "DISC IN" signal is applied to the FFSK modem IC (IC1, pin 10), and is then detected bit synchronization detection within 16 bit.

4-5-3 ENCODEING CIRCUIT

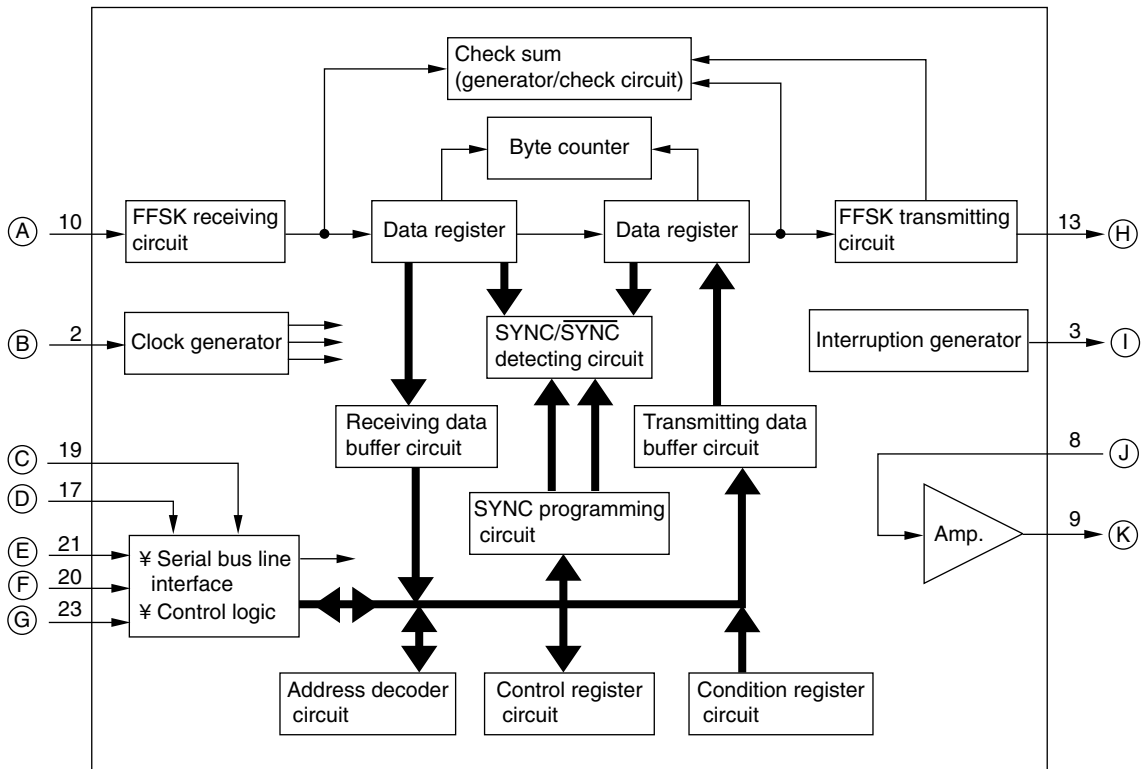
The 8 bit FFSK signal is made by serial data bus line signals, and is then output from the FFSK modem IC (IC1, pin 13).

In case of the FFSK signal is used for the PM modulation, the FM/PM switch (IC2) is switched to pin 7.

In case of the FFSK signal is used for the FM modulation, the FM/PM switch (IC2) is switched to pin 6.

The output signal from IC2, pin 1 is applied to the IC1's amplifier function (pin 8). The amplified signal is output from pin 9, and is then applied to the IC22, pin 4 (IC-F1610's MAIN unit) as "SIG OUT" signal. The signal is amplified at the buffer amplifier (IC-F1610's MAIN unit; IC503, pin 3), and is applied to the D/A convertor IC (IC-F1610's MAIN unit; IC5, pin 4). The signal is applied to the amplifier (IC-F1610's MAIN unit; Q52), and is then applied to the IC-F1610's modulation circuit (IC-F1610's MAIN unit; Q23, D21, D22, D42, D43) via the "MOD" signal.

• UT-103 BLOCK DIAGRAM



- | | |
|---------------------------|---------------------------|
| (A) : Receiving signal | (H) : Transmitting signal |
| (B) : Clock signal | (I) : IRQ signal |
| (C) : Chip select signal | (J) : Amplifier input |
| (D) : Reply data signal | (K) : Amplifier output |
| (E) : Serial clock signal | |
| (F) : Command data signal | |
| (G) : Wake signal | |

4-6 PORT ALLOCATIONS

CPU (MAIN UNIT; IC20)

Pin number	Port name	Description
20	PTTO	Outputs the PTT control signal. Low : While transmitting
21	PTTI	Input port for the PTT control signal from PTTO port.
22	AFON	Input port for the AF amplifier ON signal from an optional unit.
24	BUSY	Outputs busy signal for an optional unit.
25	POSW	Input port for the power switch. Low : While power switch is pushed
30	MMUT	Input port for microphone audio mute control signal from an optional unit.
31	RMUT	Input port for receive audio mute control signal from an optional unit.
32	NOIS	Input port for noise signals (pulse-type) for noise squelch operation.
38	AFV	Input port for the volume control.
40	RSSI	Input port for receiving signal strength level detection.
43	CDEC	Input port for CTCSS/DTCS decoding.
44	CENC	Output ports for CTCSS/DTCS signals.
47, 48	ECS2, ECS1	Output ports for EEPROM select signals. ECS1: For internal EEPROM (IC27) ECS2: For optional EEPROM
49	ECK	Outputs clock signal for EEPROMs.
50	ESI	Input port for serial signal from EEPROMs.
51	ESO	Outputs serial signal for EEPROMs.
53	BEEP	Outputs beep audio signals.
55	MCON	Outputs mic. audio mute control signal to the audio switch (IC25). High : While DTMF signals are being transmitted, etc.
56	AMUT	Outputs the AF mute switch (Q6) control signal. High : While squelched, etc.
25	NWC	Outputs N/W switch control signals. High : While wide is selected
57	HFSW	Outputs high-pass filter's characteristics select signal. High : During CTCSS operation
60	PA	Outputs mic. audio select signal to the audio switch (IC25). High : While "Public-address" function is ON
62	TMUT	Outputs MT8V regulator circuit (Q38, D27) control signal. High : While transmit is muted.

Pin number	Port name	Description
64	DSTB	Outputs strobe signals for the level controller. (IC5)
65	DDA	Outputs data signal for the level controller (IC5).
66	DCK	Outputs clock signal for the level controller (IC5).
67	PSTB	Outputs strobe signals for the PLL IC (IC12).
68	PDA	Outputs data signal for the PLL IC (IC12).
69	PCK	Outputs clock signal for the PLL IC (IC12).
72	UNLK	Input port for the PLL unlock signal. High : During unlock
73	PLLT	Outputs PLL accelerator control signal. High : While scanning, etc.
75	VTX	Outputs the T8V regulator circuit (Q38, D28) control signal. Low : While transmitting
76	VRX	Outputs the R8V regulator circuit (Q36, D27) control signal. Low : While receiving
77	PWON	Outputs the power control circuit (Q12) control signal. High : During power ON
78	PASP	Outputs "Public-address" mute signal. High : While PA and Ext. SP functions are not used
79	SP	Outputs the mute switch (Q7) control signal (incl. beep). High : While squelched, etc.
80	DIM	Input port for an external LCD backlight brightness control signal. Low : LCD backlight is dimmed
82-89	DTR1-DTR4, DTC4-DTC1	Outputs DTMF audio signals.
93	HORN	Outputs high level control signal for the pre-set time to the connected external unit when matched 2- or 5-tone code is received.
99	SIFT	Outputs CPU clock shift signal.

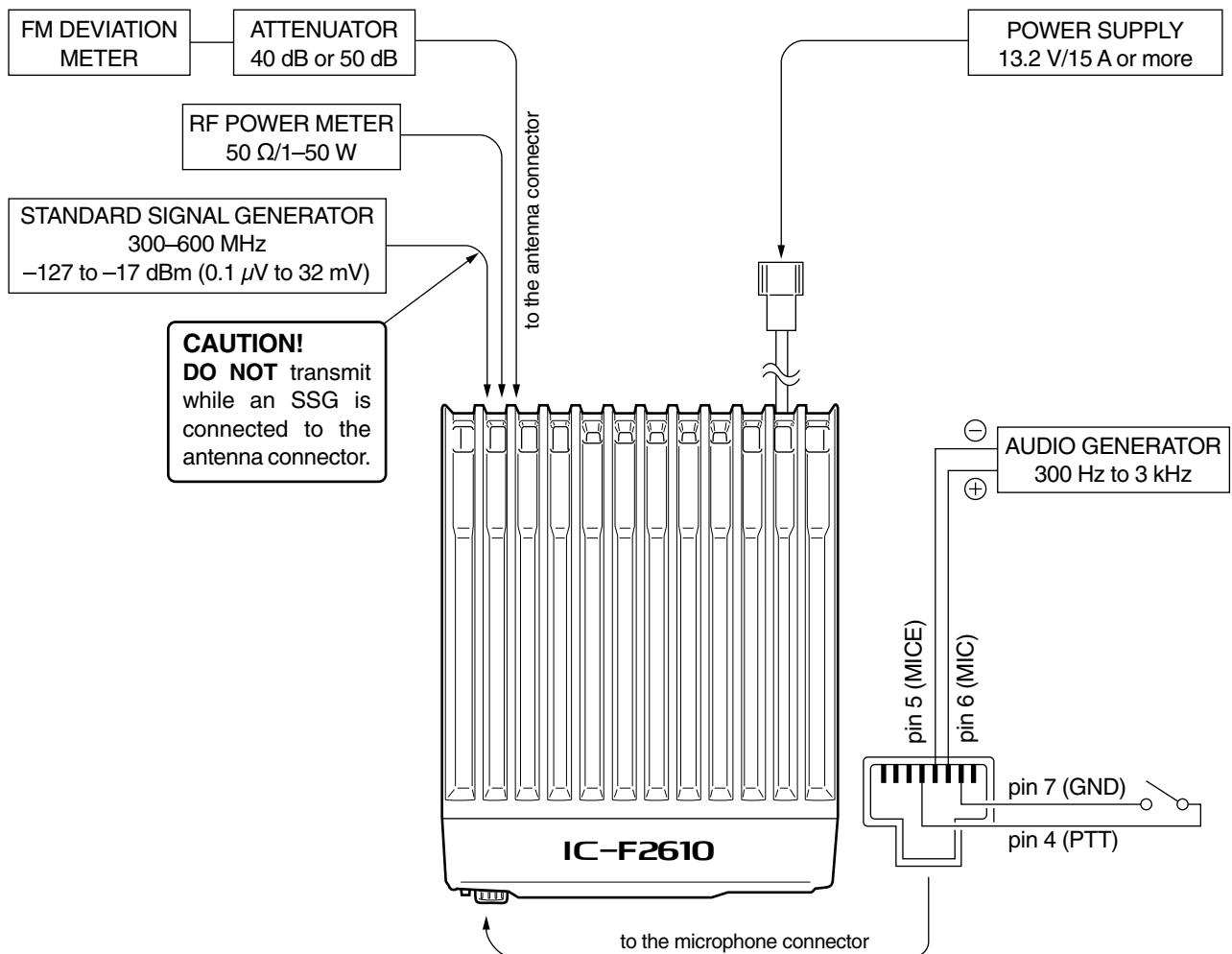
SECTION 5 ADJUSTMENT PROCEDURES

5-1 PREPARATION

■ REQUIRED TEST EQUIPMENT

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output Voltage : 13.2 V DC Current capacity : 15 A or more	Standard signal generator (SSG)	Frequency range : 0.1–600 MHz Output level : 0.1 μ V–32 mV (–127 to –17 dBm)
RF power meter (terminated type)	Measuring range : 1–50 W Frequency range : 300–600 MHz Impedance : 50 Ω SWR : Less than 1.2 : 1	Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–20 V
Frequency counter	Frequency range : 0.1–600 MHz Frequency accuracy: \pm 1 ppm or better Sensitivity : 100 mV or better	DC voltmeter	Input impedance : 50 k Ω /V DC or better
RF voltmeter	Frequency range : 0.1–600 MHz Measuring range : 0.01–10 V	Digital multimeter	Measuring range : 10 mV–10 V
FM deviation meter	Frequency range : DC–600 MHz Measuring range : 0 to \pm 10 kHz	AC millivoltmeter	Input impedance : 10 M Ω /V DC or better
Audio generator	Frequency range : 300–3000 Hz Measuring range : 1–500 mV	External speaker	Input impedance : 4 Ω Capacity : 5 W or more
		Attenuator	Power attenuation : 40 dB or 50 dB Capacity : 50 W or more
		Terminator	Impedance : 50 Ω Capacity : 50 W or more

■ CONNECTION



5-2 INITIAL SET MODE

The following items can be adjusted via *Initial Set Mode* without opening the transceiver's case.

■ ENTERING INITIAL SET MODE

- ① Turn the transceiver power OFF.
- ② While pushing \triangle and ∇ , turn power ON.
 - Bank number appears regardless of the channel separation type, 'bank' or 'free'.
- ③ Push P_0 to cycle through the initial set mode items.

NOTE: Initial Set Mode access can be inhibited through PC programming. In such case, P_0 cannot be used and only 'DISPLAY' setting is available. Ask your Dealer or Icom Service Center for PC programming.

■ SELECTABLE ITEMS

No.	ITEM	SELECTABLE CONDITIONS		
		P_1	P_2	P_3
1	DISPLAY	Backlight	—	Contrast
2	AF/SQUELCH	—	Squelch level	Minimum AF level
3	BEEP TONES	Link ON/OFF	Beep tones ON/OFF	Beep level
4	DEVIATION	DTCS balance	Tone deviation	Max. voice deviation
5	S-METER	Indicate the received signal level regardless of P_1 to P_3 keys.		
6	TX POWER	Low 1	Low 2	High

■ SELECTION METHOD

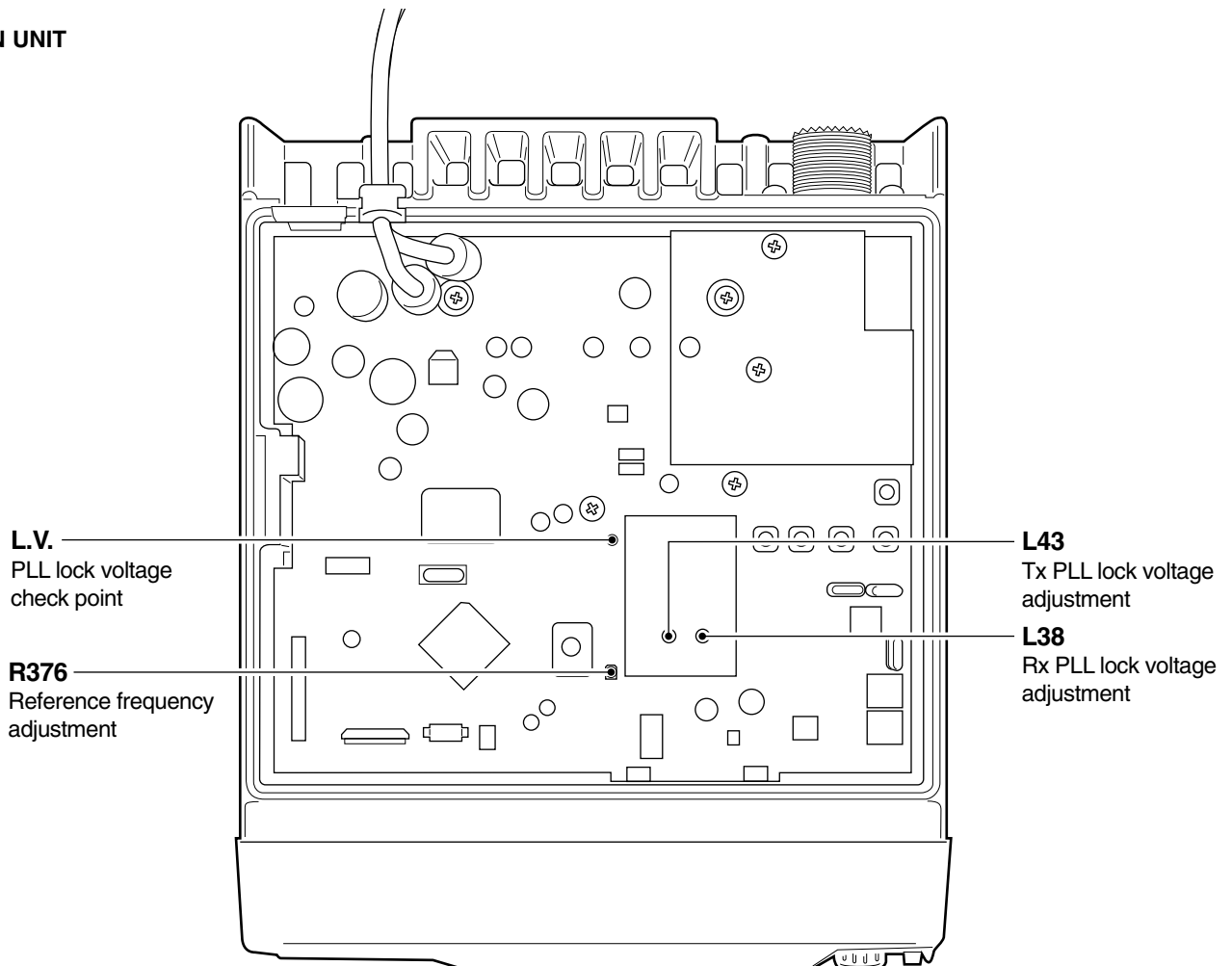
MODE No.	ITEM	METHOD	NOTE
1	Display backlight	Push P_1 to select 'bright', 'dark' or 'off'.	
	Display contrast	Rotate the volume control while pushing P_3 .	
2	Squelch level	Rotate the volume control while pushing P_2 .	
	Minimum AF level	Rotate the volume control while pushing P_3 .	
3	Link/unlink beep tones with the volume control	Push P_1 to select 'link' or 'unlink'.	2 beeps: link 1 beep: unlink
	Beep ON/OFF	Push P_2 to turn beeps ON and OFF.	2 beeps: ON 1 beep: OFF Effective after exiting Initial Set Mode
	Maximum beep level	Push P_3 to select the desired beep level.	
4	DTCS balance	Rotate the volume control while pushing P_1 .	Automatic transmission while pushing the key.
	CTCSS/DTCS Tone deviation	Rotate the volume control while pushing P_2 .	Automatic transmission while pushing the key. Separate setting for CTCSS and DTCS depending on the programmed tone system.
	Maximum voice deviation	Rotate the volume control while pushing P_3 .	Automatic transmission while pushing the key.
5	S-meter level	—	Received signal level is shown in the display.
6	Transmit low power (L1)	Rotate the volume control while pushing P_1 .	Automatic transmission while pushing the key.
	Transmit low power (L2)	Rotate the volume control while pushing P_2 .	Same as above.
	Transmit high power (H)	Rotate the volume control while pushing P_3 .	Same as above.

5-3 PLL ADJUSTMENT


ADJUSTMENT	ADJUSTMENT CONDITIONS	MEASUREMENT		VALUE	ADJUSTMENT		
		UNIT	LOCATION		UNIT	ADJUST	
PLL LOCK VOLTAGE	1 • Operating freq. : 390.000 MHz [L] 440.000 MHz [M] 480.000 MHz [H] • Receiving	MAIN	Connect a digital multi-meter or an oscilloscope to the check point "LV".	2.0 V	MAIN	L38	
	2 • Operating freq. : 430.000 MHz [L] 490.000 MHz [M] 520.000 MHz [H] • Receiving					7.0–13.0 V	Verify
	3 • Operating freq. : 390.000 MHz [L] 440.000 MHz [M] 480.000 MHz [H] • Transmitting					2.0 V	L43
	4 • Operating freq. : 430.000 MHz [L] 490.000 MHz [M] 520.000 MHz [H] • Transmitting					7.0–13.0 V	Verify
PLL REFERENCE FREQUENCY	1 • Operating freq. : 390.000 MHz [L] 440.000 MHz [M] 480.000 MHz [H] • Transmitting	Rear panel	Loosely couple a frequency counter to the antenna connector.	390.0000 MHz [L] 440.0000 MHz [M] 480.0000 MHz [H]	MAIN	R376	

[L]: [L-band (400–430 MHz)], [M]: [M-band (440–490 MHz)], [H]: [H-band (490–520 MHz)]

• MAIN UNIT



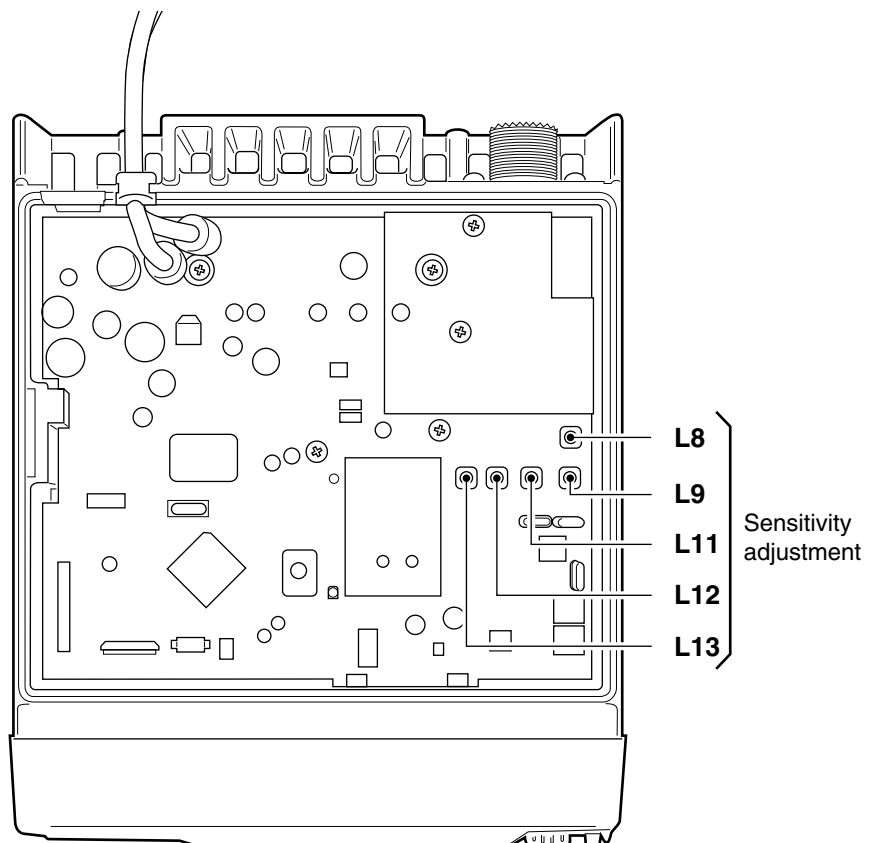
5-4 RECEIVER ADJUSTMENT

ADJUSTMENT	ADJUSTMENT CONDITIONS	MEASUREMENT METHOD	ADJUSTMENT	
			VALUE	ADJUST
RECEIVER SENSITIVITY	1 <ul style="list-style-type: none"> Operating freq. : 400.000 MHz [L] 440.000 MHz [M] 490.000 MHz [H] Enter Initial Set Mode No. 5. Refer to page 5-2 for details. Connect a standard signal generator to the antenna connector and set as: Level : 5.6 μV* (-92 dBm) Modulation : OFF Connect a 4 Ω load to the external speaker jack. Receiving 	Number digits in the LCD 	Maximum indication	Adjust in sequence L8, L9, L11, L12, L13 on the MAIN unit.
NOISE SQUELCH THRESHOLD POINT	1 <ul style="list-style-type: none"> Operating freq. : 400.000 MHz [L] 440.000 MHz [M] 490.000 MHz [H] Enter Initial Set Mode No. 2. Refer to page 5-2 for details. Make sure no signal is being applied to the antenna connector. Receiving 	Speaker output	At the point where the noise audio just disappears.	Rotate volume control while pushing P2 .
	2 <ul style="list-style-type: none"> Connect an SSG to the antenna connector and set as: Level : 0.32 μV* (-117 dBm) Deviation : \pm3.5 kHz Modulation : 1 kHz Receiving 		Squelch opens.	Verify
BEEP LEVEL	1 <ul style="list-style-type: none"> Operating freq. : Any Enter Initial Set Mode No. 3. Refer to page 5-2 for details. Receiving 	Speaker output	Desired level	Push P3 to select the beep level.

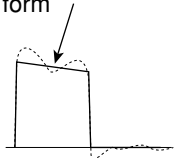
*This output level of the standard signal generator (SSG) is indicated as SSG's open circuit.

[L]: [L-band (400–430 MHz)], [M]: [M-band (440–490 MHz)], [H]: [H-band (490–520 MHz)]

• MAIN UNIT



5-5 TRANSMITTER ADJUSTMENT

ADJUSTMENT	ADJUSTMENT CONDITIONS	MEASUREMENT METHOD	ADJUSTMENT	
			VALUE	ADJUST
OUTPUT POWER	<ul style="list-style-type: none"> Operating freq. : 400.000 MHz [L] 440.000 MHz [M] 490.000 MHz [H] 465.000 MHz [[EUR-13], [[EUR-02], [EUR-72] only Enter Initial Set Mode No. 6. Refer to page 5-2 for details. 	Connect an RF power meter to the antenna connector.	24 W [25 W] 10 W [10 W]	Rotate volume control while pushing (P3) .
			10 W [25 W] 5 W [10 W]	Rotate volume control while pushing (P2) .
			2.5 W	Rotate volume control while pushing (P1) .
NOTE: When the RF output power cannot be set with this procedure, cloning may be necessary to cancel the output power setting.				
FM DEVIATION	<ul style="list-style-type: none"> Operating freq. : 400.000 MHz [L] 440.000 MHz [M] 490.000 MHz [H] Enter Initial Set Mode No. 4. Refer to page 5-2 for details. Connect an audio generator to the microphone connector and set as: 1 kHz/35 mV Set an FM deviation meter as: HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P-P)/2 W/N setting : Wide 	Connect an FM deviation meter to the antenna connector through an attenuator.	±4.0 kHz [W]	Rotate volume control while pushing (P3) .
	<ul style="list-style-type: none"> W/N setting : Narrow 		±2.0 kHz [N]	
DTCS WAVE FORM AND DEVIATION	<ul style="list-style-type: none"> Operating freq. : 415.000 MHz [L] 465.000 MHz [M] 505.000 MHz [H] Enter Initial Set Mode No. 4. Refer to page 5-2 for details. No AF signals are applied to the microphone connector. 	Connect an FM deviation meter with an oscilloscope to the antenna connector through an attenuator.	Set to flat wave form 	Rotate volume control while pushing (P1) .
	<ul style="list-style-type: none"> Set an FM deviation meter as: HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P-P)/2 W/N setting : Wide DTCS code : 007 		±0.7 kHz [W]	Rotate volume control while pushing (P2) .
	<ul style="list-style-type: none"> W/N setting : Narrow 		±0.35 kHz [N]	
CTCSS TONE DEVIATION	<ul style="list-style-type: none"> Operating freq. : 415.000 MHz [L] 465.000 MHz [M] 505.000 MHz [H] Enter Initial Set Mode No. 4. Refer to page 5-2 for details. No AF signals are applied to the microphone connector. Set an FM deviation meter as: HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P-P)/2 W/N setting : Wide CTCSS tone freq. : 88.5 Hz 	Connect an FM deviation meter to the antenna connector through an attenuator.	±0.7 kHz [W]	Rotate volume control while pushing (P2) .
	<ul style="list-style-type: none"> W/N setting : Narrow 		±0.35 kHz [N]	

[L]: [L-band (400–430 MHz)], [M]: [M-band (440–490 MHz)], [H]: [H-band (490–520 MHz)], [W]: 25 kHz, [N]: 12.5 kHz

[MAIN UNIT]

Table with columns: REF NO., ORDER NO., DESCRIPTION, M. Contains component data for the MAIN UNIT.

[MAIN UNIT]

Table with columns: REF NO., ORDER NO., DESCRIPTION, M. Contains component data for the MAIN UNIT.

Ⓐ: [EUR-01], [EUR-02], [EUR-71], [EUR-72]

Ⓒ: [EUR-2], [EUR-4], [EUR-6], [EUR-7], [EUR-9], [EUR-11], [EUR-14]

Ⓔ: [EUR-1], [EUR-5], [EUR-8]

Ⓛ: [EUR-8], [EUR-9], [EUR-10], [EUR-11]

Ⓚ: [400-430 MHz]

Ⓞ: [10 W version]

Ⓡ: [EUR-01], [EUR-02], [EUR-12], [EUR-13], [EUR-71], [EUR-72]

Ⓢ: [EUR-02], [EUR-13], [EUR-72]

Ⓣ: [EUR-5], [EUR-6], [EUR-7]

Ⓤ: [EUR-12], [EUR-13], [EUR-14]

Ⓝ: [440-490 MHz]

Ⓔ: [EUR-01], [EUR-12], [EUR-71]
Ⓝ: [490-520 MHz]

Ⓚ: [EUR-01], [EUR-02]

Ⓝ: [EUR-71], [EUR-72]

[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION		M.
C608	4030009530	S.CERAMIC	C1608 CH 1H 030B-T	Ⓑ only T
C609	4030009530	S.CERAMIC	C1608 CH 1H 030B-T	Ⓑ only B
C610	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only B
C611	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only B
C612	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only B
C613	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only T
C614	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only B
C615	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only T
C616	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only B
C617	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only B
C618	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only B
C619	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only B
C620	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only B
C621	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only B
C622	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only B
C623	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only T
C624	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only T
C625	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only B
C626	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only B
C627	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only B
C628	4030007050	S.CERAMIC	C1608 CH 1H 220J-T	Ⓑ only T
C629	4030009500	S.CERAMIC	C1608 CH 1H 0R5B-T	Ⓓ only B
C630	4030007110	S.CERAMIC	C1608 CH 1H 680J-T	Ⓑ only B
J2	6450000140	CONNECTOR	HSJ0807-01-010	B
J4	6510019250	S.CONNECTOR	B11B-ZR-SM3-TF	T
J5	6510018040	CONNECTOR	52330-1217	T
J6	6510018430	S.CONNECTOR	AXN330C038P	T
J7	6510019270	S.CONNECTOR	52365-0691	T
J501	6510021300	S.CONNECTOR	52365-1091	T
W3	7030003860	S.RESISTOR	ERJ3GE JPW V	B
W4	8900004540	CABLE	OPC-453	T
W6	7120000470	JUMPER	ERDS2T0	T
W11	7030003860	S.RESISTOR	ERJ3GE JPW V	Ⓐ only T
W12	7030003860	S.RESISTOR	ERJ3GE JPW V	Ⓜ only T
W13	7030003860	S.RESISTOR	ERJ3GE JPW V	ⓗ only T
W14	7030003860	S.RESISTOR	ERJ3GE JPW V	Ⓒ only T
W21	7030003860	S.RESISTOR	ERJ3GE JPW V	Ⓔ only T
W25	7030003860	S.RESISTOR	ERJ3GE JPW V	Ⓘ only T
W26	7030003860	S.RESISTOR	ERJ3GE JPW V	Ⓙ only T
W27	7030003860	S.RESISTOR	ERJ3GE JPW V	Ⓚ only T
W28	7030003860	S.RESISTOR	ERJ3GE JPW V	Ⓝ only T
W505	7030003860	S.RESISTOR	ERJ3GE JPW V	B
W506	7030003860	S.RESISTOR	ERJ3GE JPW V	B
W507	7030003860	S.RESISTOR	ERJ3GE JPW V	Ⓛ, Ⓟ, Ⓝ only T
W508	7030003860	S.RESISTOR	ERJ3GE JPW V	B
W509	7030003860	S.RESISTOR	ERJ3GE JPW V	T
W510	7030003860	S.RESISTOR	ERJ3GE JPW V	Ⓑ only B
W511	7030003860	S.RESISTOR	ERJ3GE JPW V	Ⓑ only T
EP1	0910051253	PCB	B 5204C	[Other]
	0910054832	PCB	B 5791B	Ⓑ
EP2	6910010220	BEAD	HF70BB3.5X5X1.3	T
EP3	6910010280	BEAD	HF70BB9.5X10.4X4.9	T
EP4	0880000270	UNIT BOARD	EX-1804 #02	Ⓝ only T
EP5	0880001240	UNIT BOARD	EX-1761 #02	Ⓝ only T

[TONE UNIT] (UT-96 pre-installed version ONLY)

REF NO.	ORDER NO.	DESCRIPTION		M.
EP1	0880000150	UNIT BOARD	EX-1643 #02	T

Ⓐ: [EUR-01], [EUR-02], [EUR-71], [EUR-72]

Ⓑ: [EUR-2], [EUR-4], [EUR-6], [EUR-7], [EUR-9], [EUR-11], [EUR-14]

Ⓒ: [EUR-1], [EUR-5], [EUR-8]

Ⓓ: [EUR-8], [EUR-9], [EUR-10], [EUR-11]

Ⓔ: [400-430 MHz]

Ⓛ: [10 W version]

Ⓜ: [EUR-01], [EUR-02], [EUR-12], [EUR-13], [EUR-71], [EUR-72]

Ⓨ: [EUR-02], [EUR-13], [EUR-72]

Ⓩ: [EUR-5], [EUR-6], [EUR-7]

Ⓚ: [EUR-12], [EUR-13], [EUR-14]

Ⓜ: [440-490 MHz]

Ⓟ: [EUR-01], [EUR-71]

ⓗ: [490-520 MHz]

Ⓚ: [EUR-01], [EUR-02]

Ⓝ: [EUR-71], [EUR-72]

M.=Mounted side (T: Mounted on the Top side, B: Mounted on the Bottom side)

S.=Surface mount

SECTION 7 MECHANICAL PARTS AND DISASSEMBLY

[CHASSIS PARTS]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
J1	6510004880	Connector MR-DS-E 01	1
MP1	8010019000	1705 chassis (B)-1	1
MP2	8810008660	Screw PH BT M3 × 8 NI-ZU	4
MP3	8810008660	Screw PH BT M3 × 8 NI-ZU	2
MP4	8810008660	Screw PH BT M3 × 8 NI-ZU	2
MP5	8810009370	Screw PH BT M3 × 12 ZK	4
MP6	8930027480	1126 TR-A clip	1
MP7	8820000870	1705 cap screw	3
MP8	8110006941	1705 cover (B)-1	1
MP11	8930039611	Thermally sheet (C)-1	1
MP15	8930039630	1706 jack sheet	1
MP16	8930036771	1705 main seal-1	1
MP17	8930056200	Shield tape (K) [R&TTE] only	1
MP18	8930056000	Shield tape (I) [R&TTE] only	1
MP20	8930037760	Insulation plate	1

[FRONT UNIT]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
R26	7210002830	EVU-F2JFK4 B14	1
J1	6450001470	Connector 95003-2881	1
DS1	5030002180	LCD TSC0712-UFTDHW	1
EP2	8930048320	LCD contact SRCN-2140-SP-N-W	2
MP1	8210015740	2140 front panel assembly	1
MP2	8930047980	2140 LCD holder	1
MP3	8930048290	2140 LCD filter	1
MP4	8210015770	2140 reflector	1
MP5	8930059320	2140 front key (B) [BIIS]only	1
	8930047860	2140 front key [OTHER]	1
MP7	8610009840	Knob N234	1
MP9	8810008760	Screw PH BT M2 × 8 NI-ZU	5
MP10	8930048910	2140 earth plate	1
MP11	8930049640	2141 plate	1

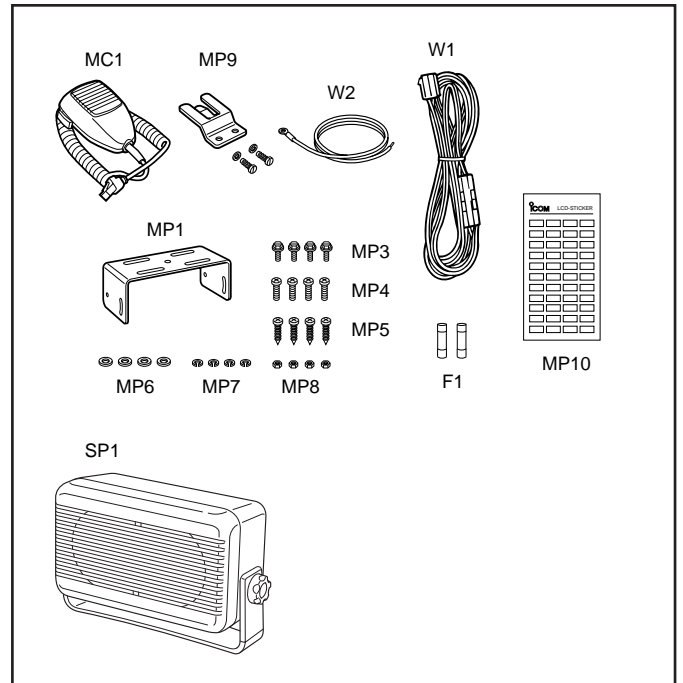
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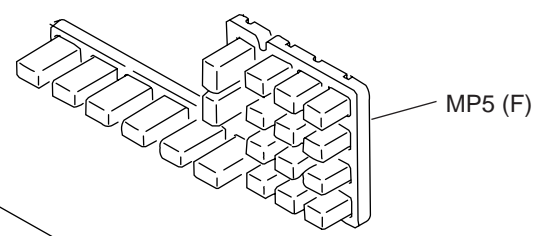
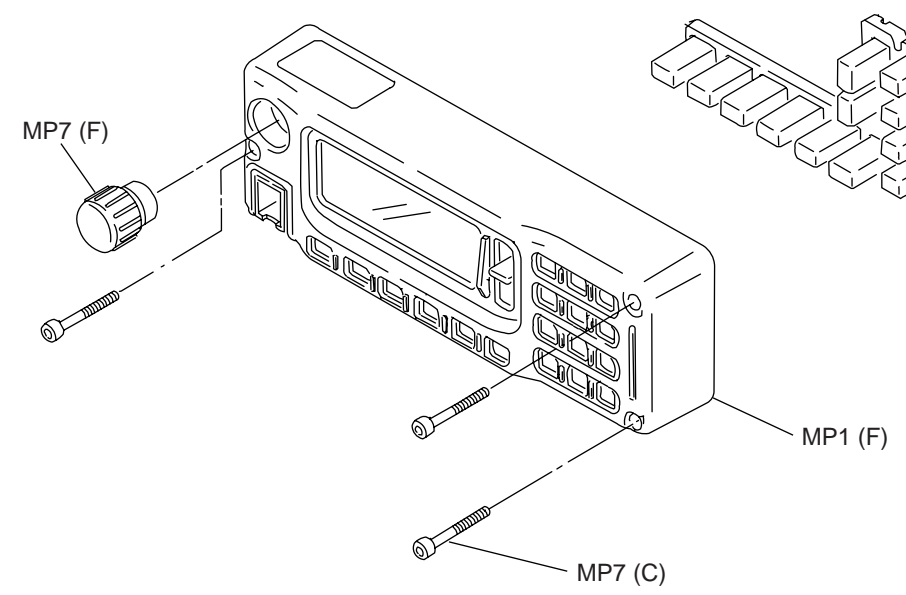
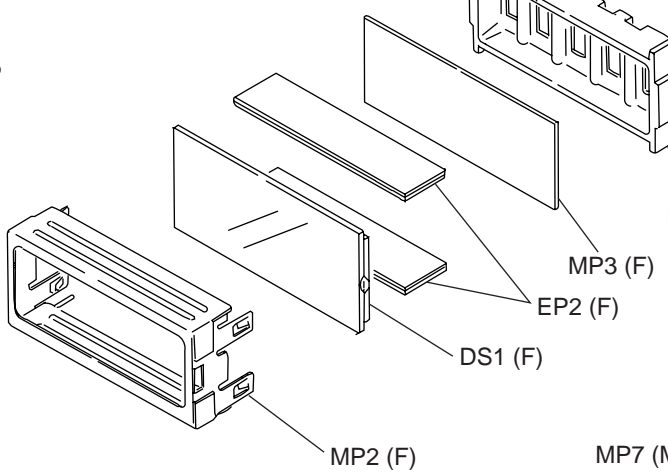
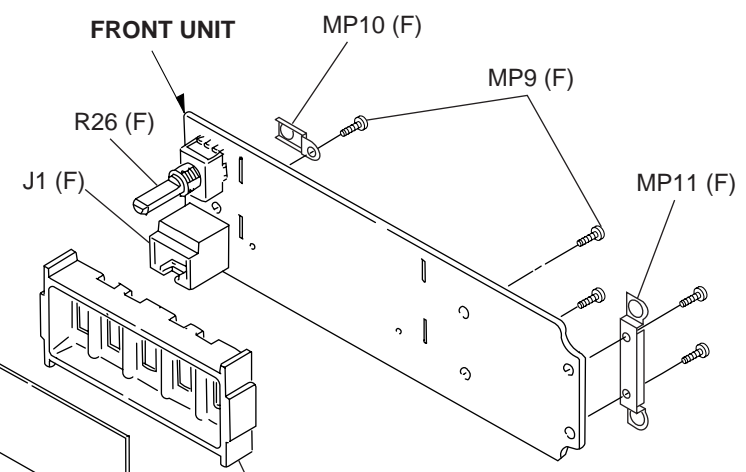
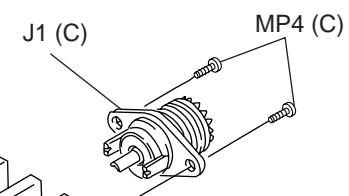
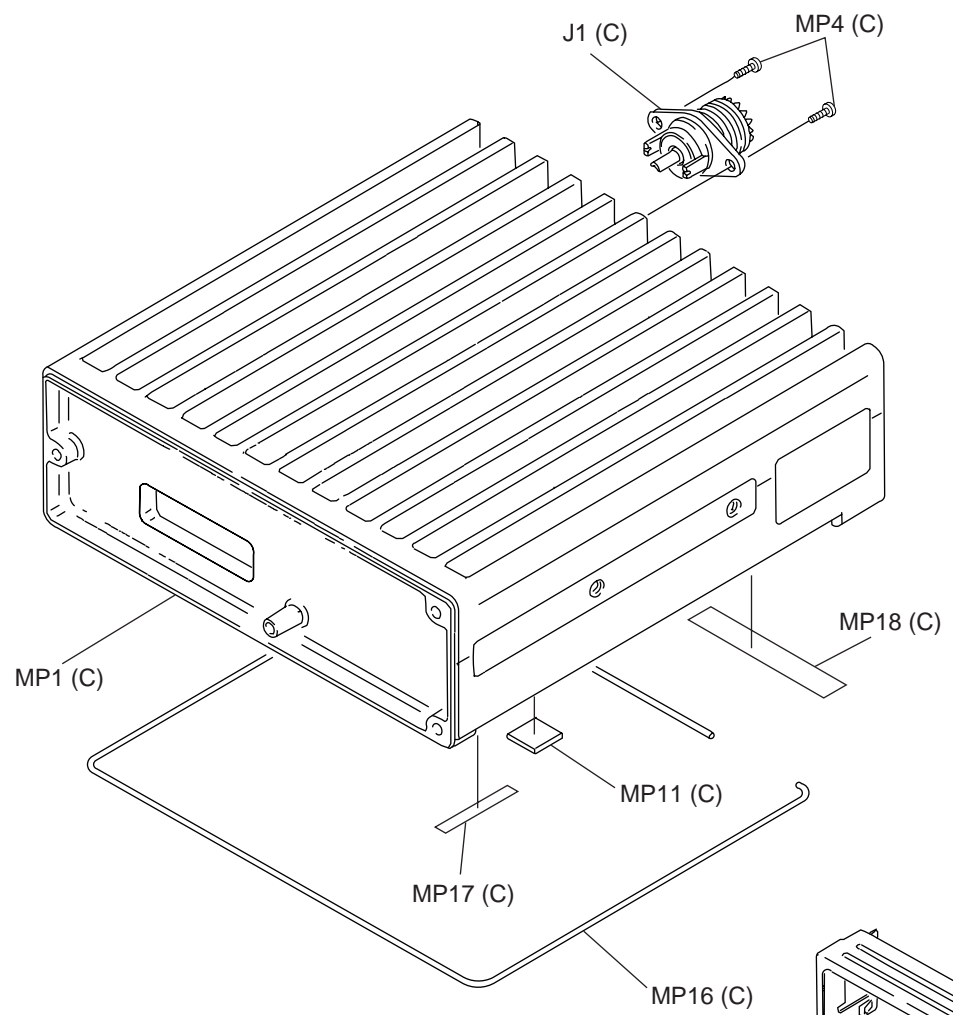
REF. NO.	ORDER NO.	DESCRIPTION	QTY.
J2	6450000140	Connector HJSJ0807-01-010	1
J5	6510018040	Connector 52330-1217	1
W4	8900004540	Cable OPC-453	1
MP1	8510006810	DC-DC case	1
MP2	8510009980	1705 VCO case	1
MP4	8510010080	1705 VCO cover	1
MP6	8930037840	1705 connector spring	1
MP7	8510005070	599 shield plate	1
MP8	8510010240	1705 LPF cover	1
MP9	8510010230	1705 LPF case	1
MP10	8510010250	1705 shield plate	1
MP11	8930029511	1327 ANT plate-1	1
MP12	8930038790	1706 spring	1
MP13	8930049590	Sheet (G)	2
MP14	8930057730	Shield sponge (J) [R&TTE] only	1
MP15	8930057730	Shield sponge (J) [R&TTE] only	1
MP16	8930056180	1706 rear spring [R&TTE] only	1
MP17	8930056180	1706 rear spring [R&TTE] only	1
MP18	8930056180	1706 rear spring [R&TTE] only	1
MP19	8930001160	Earth spring [R&TTE (Middle-band)] only	1
MP20	8930005320	Filter spacer	2

[ACCESSORIES]

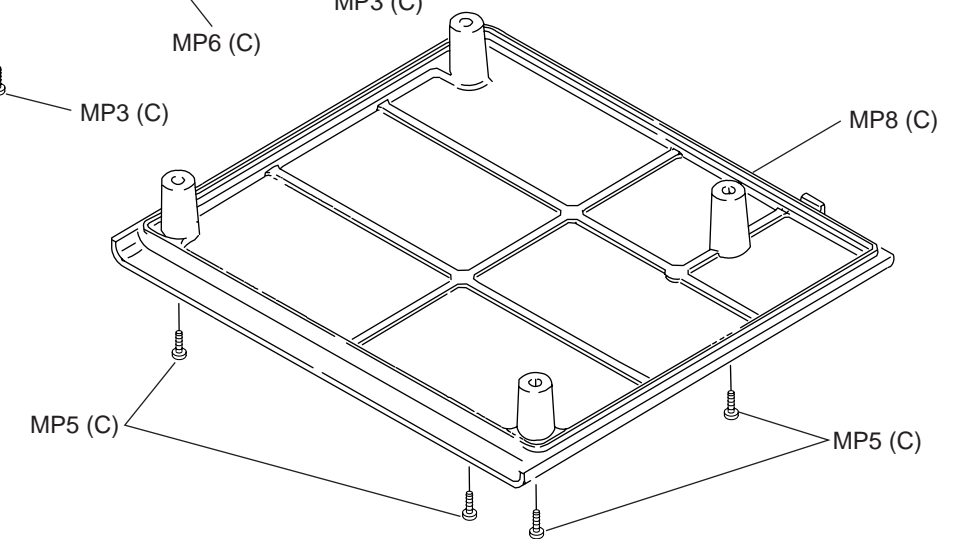
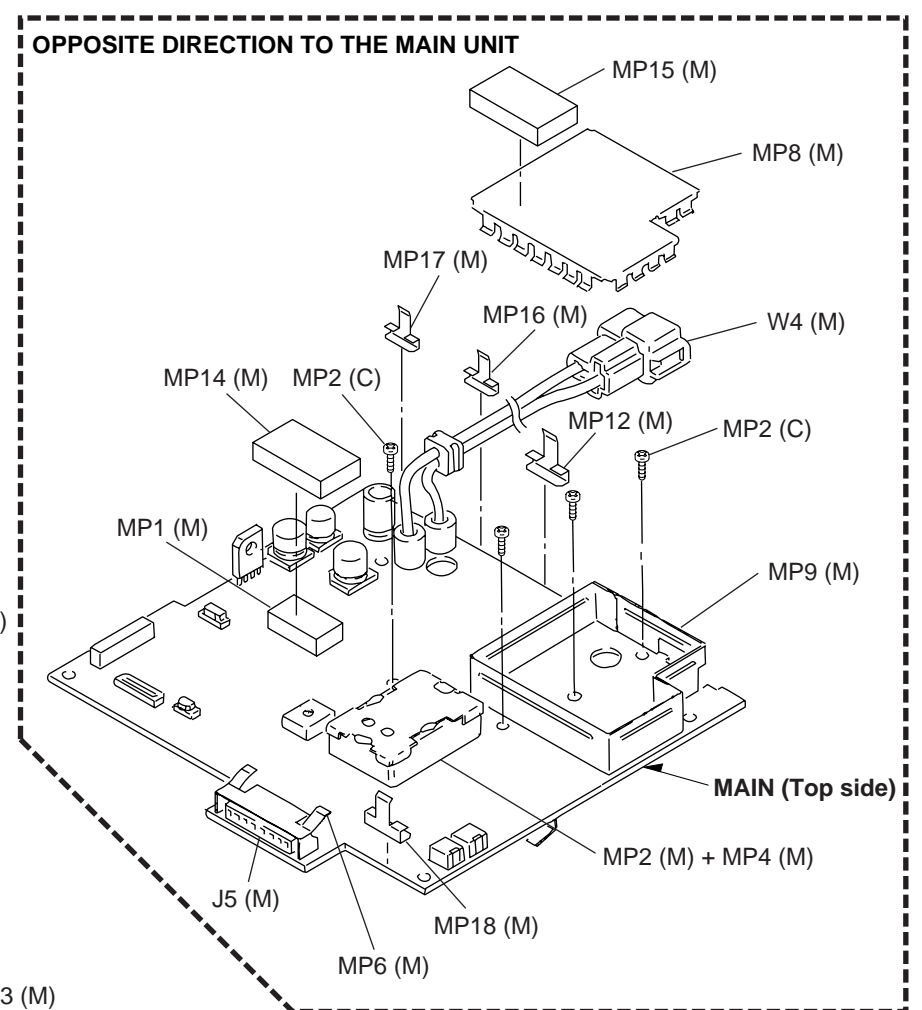
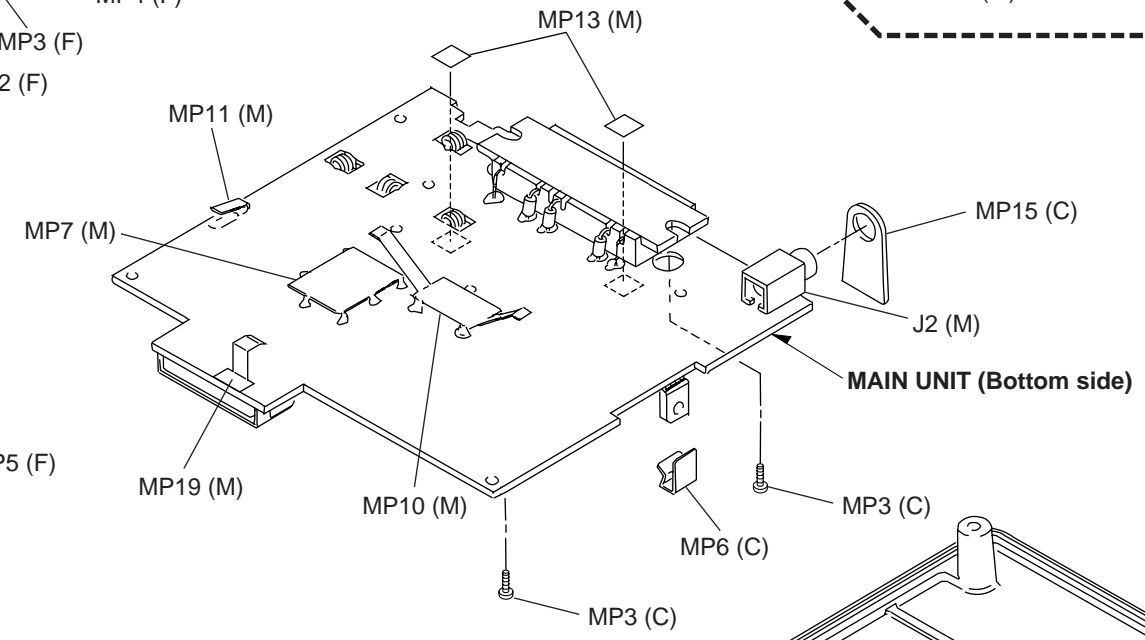
REF. NO.	ORDER NO.	DESCRIPTION	QTY.
F1	5210000120	Fuse FGB 15A	2
MC1	0800005780	Microphone HM-100N	1
SP1	0800005120	Speaker SP-22	1
W1	8900003751	Cable OPC-345	1
W2	8900000730	Cable OPC-049	1
MP1	8010016730	150 mounting bracket	1
MP3	8820000530	Flange bolt M4 × 8 NI	4
MP4	8810000470	Screw PH M5 × 12 (+-)	4
MP5	8810005840	Screw PH A M5 × 20	4
MP6	8850000150	Flat washer M5 NI BS	4
MP7	8850000390	Spring washer M5	4
MP8	8830000120	Nut M5	4
MP9	6910004210	731 MIC hanger set	1
MP10	8310054790	1705 LCD seal (G)	1

Screw abbreviations A, BT: Self-tapping
 PH: Pan head ZK: Black
 BS: Brass NI: Nickel
 NI-ZU: Nickel-Zinc



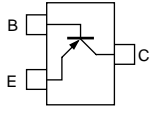
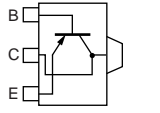
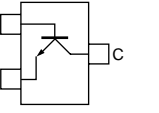
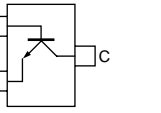
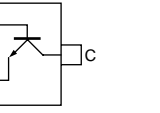
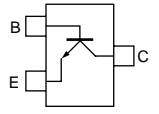
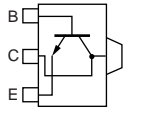
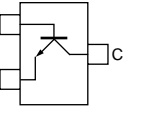
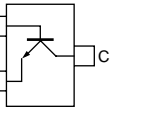
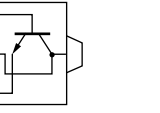
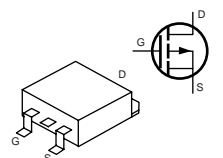
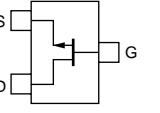
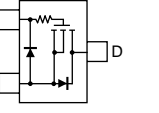
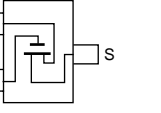
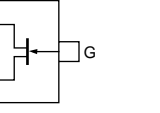
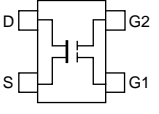
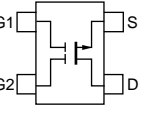
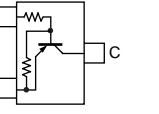
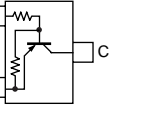
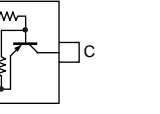
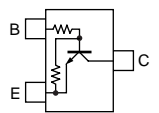
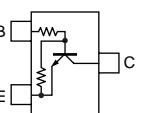
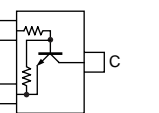
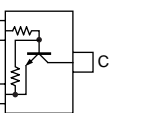
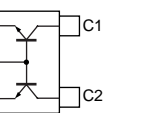
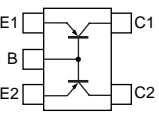
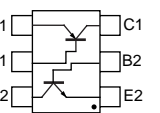


Unit abbreviations (F) : FRONT UNIT
(M) : MAIN UNIT
(C) : CHASSIS PARTS

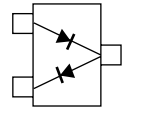
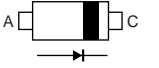
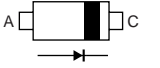


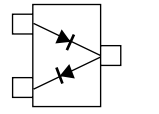
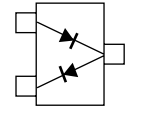
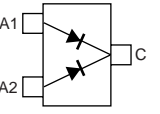
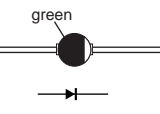
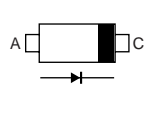
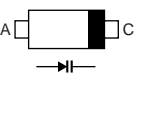
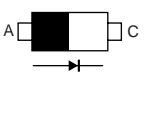
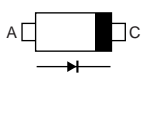
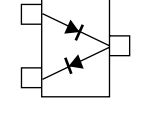
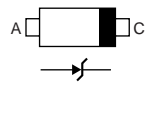
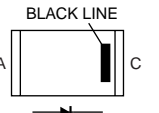


SECTION 8 SEMI-CONDUCTOR INFORMATION

• TRANSISTORS AND FET'S

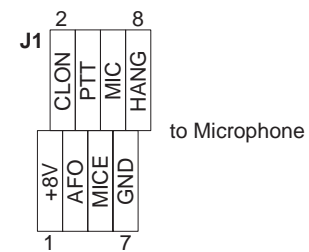
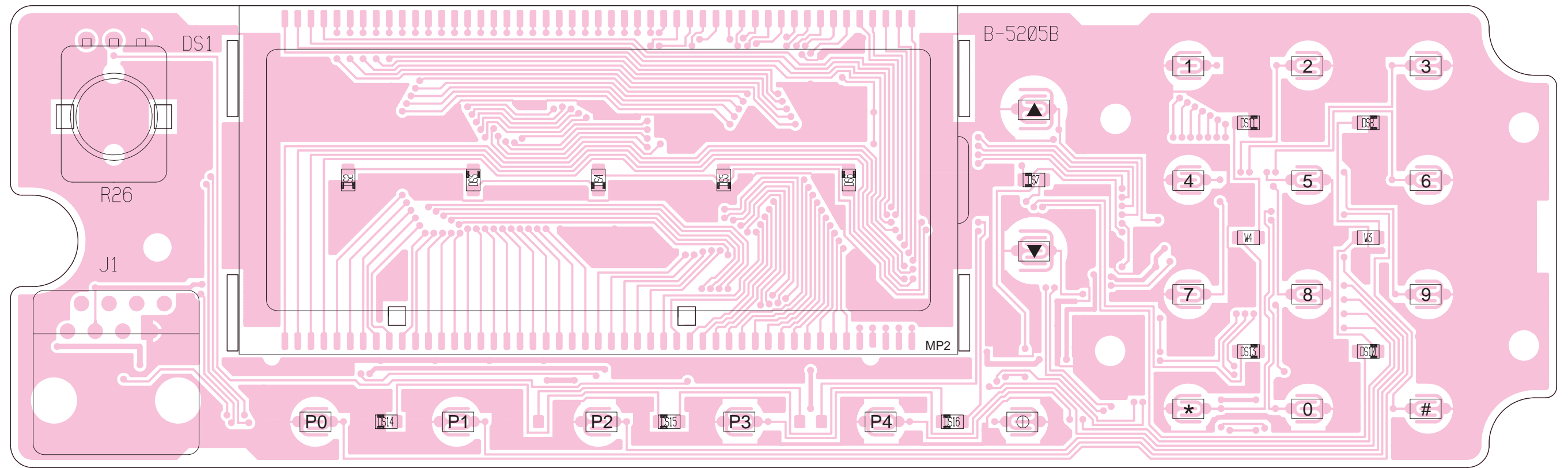
2SA1576A T106 R (Symbol: FR) 	2SB1123 T TD (Symbol: BF) 	2SC3356 T1B R25 (Symbol: R25) 	2SC4081 T106 R (Symbol: BR) 	2SC4116 BL (Symbol: LL) 
2SC4226 T1 R25 (Symbol: R25) 	2SC4703-T1 SE (Symbol: SE) 	2SC5107 O (Symbol: MFO) 	2SC5110 O (Symbol: MGO) 	2SD1664 T100Q (Symbol: DAQ) 
2SJ377 (Symbol: 4L) 	2SK1069 4 TL (Symbol: FJ) 	2SK1829 (Symbol: K1) 	2SK302 GR (Symbol: TG) 	2SK880 GR (Symbol: XG) 
3SK166A-2-T7 (Symbol: K) 	3SK206 T1 U78 (Symbol: U78) 	DTA114EUA T106 (Symbol: 14) 	DTA143ZUA T106 (Symbol: 113) 	DTA144EUA T106 (Symbol: 16) 
DTC114EUA T106 (Symbol: 24) 	DTC114YUA (Symbol: 64) 	DTC144EUA T106 (Symbol: 26_) 	DTC363 EK (Symbol: H27) 	FMS2A T148 (Symbol: S2) 
FMW2 T148 (Symbol: W2) 	XP4601 (Symbol: 5C) 			

• DIODES

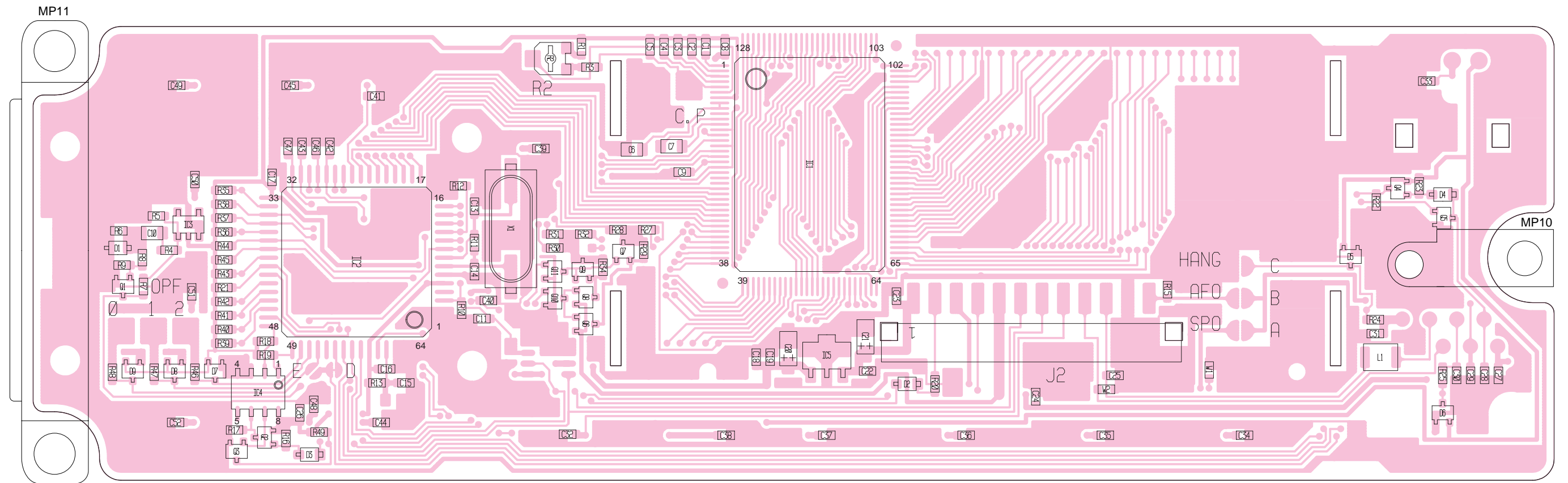
1SS302 (Symbol: C3) 	1SS352 (Symbol: C1) 	1SS355 (Symbol: A) 	1SV217 (Symbol: T6) 	1SV245 (Symbol: T3) 
DA204 U T106 (Symbol: K) 	DA221 TL (Symbol: K) 	DAN202 U T106 (Symbol: N) 	DSA3A1 (Color: Green) 	HSU88TRF (Symbol: 9) 
HVU350B TRF (Symbol: B0) 	MA77 (Symbol: 4B) 	MA111 (Symbol: 1B) 	MA742 (Symbol: M1U) 	MA8160 H (Symbol: 16^) 
UM9401F (Symbol: none) 				

SECTION 9 BOARD LAYOUTS

9-1 FRONT UNIT • TOP VIEW



• BOTTOM VIEW (FRONT UNIT)

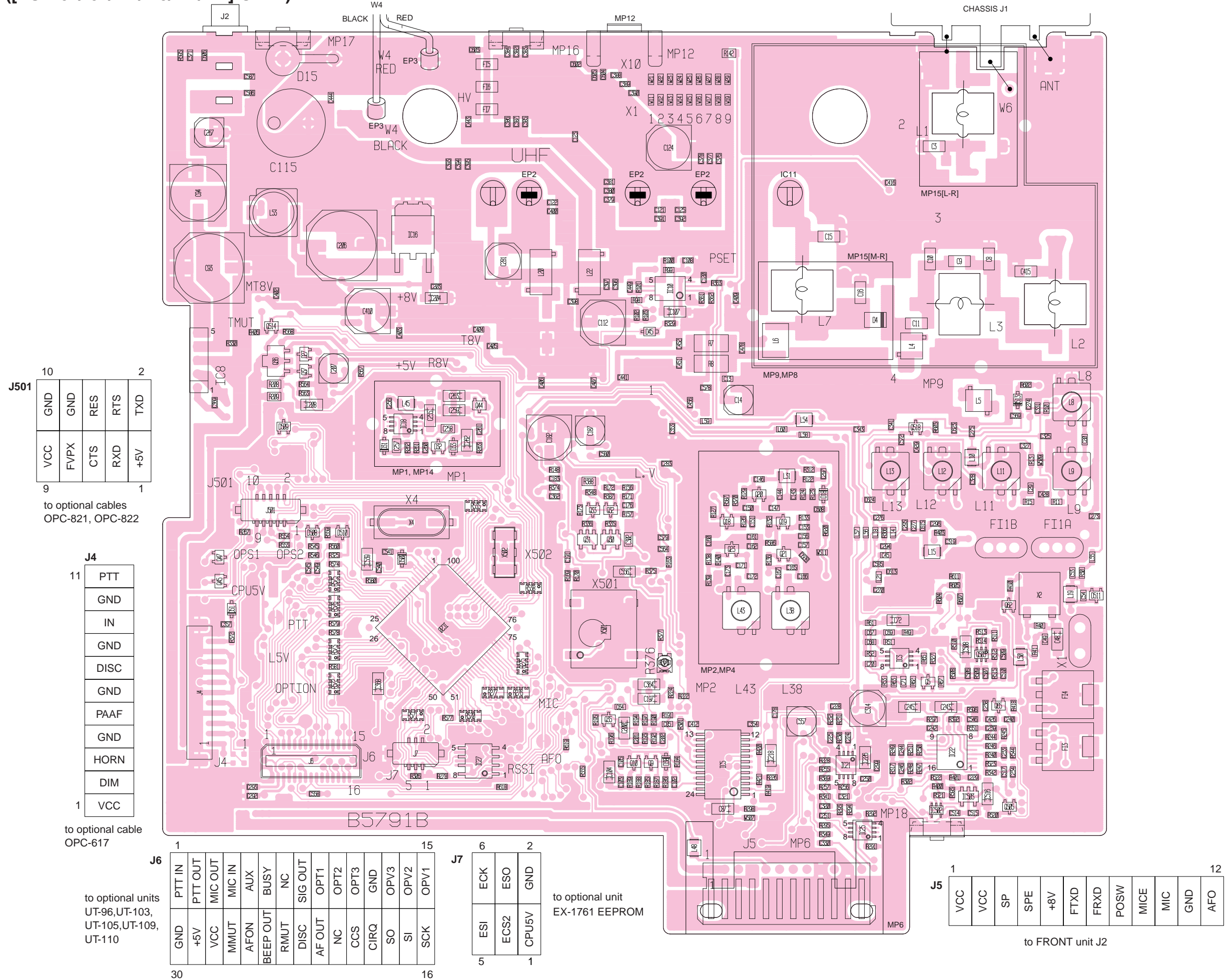


J2	1	VCC	12
		SOL	
		SP	
		SPE	
		+8V	
		FTXO	
		FRXO	
		POSW	
		MICE	
		MIC	
		GND	
		AFO	

to MAIN unit J5

9-2 MAIN UNIT ([EUR-01/-02/-12/-13/-71/-72] ONLY)

• TOP VIEW



J501

10	GND	2
	GND	
	RES	
	RTS	
	TXD	
	VCC	
	FVPX	
	CTS	
	RXD	
	+5V	
9		1

to optional cables
OPC-821, OPC-822

J4

11	PTT
	GND
	IN
	GND
	DISC
	GND
	PAAF
	GND
	HORN
	DIM
1	VCC

to optional cable
OPC-617

to optional units
UT-96, UT-103,
UT-105, UT-109,
UT-110

J6

1	PTT IN	15
	PTT OUT	
	MIC OUT	
	MIC IN	
	AUX	
	BEEP OUT	
	RMUT	
	DISC	
	SIG OUT	
	OPT1	
	OPT2	
	OPT3	
	GND	
	OPV3	
	OPV2	
	OPV1	
30		16

J7

6	ECK	2
	ESO	
	GPU5V	
5		1

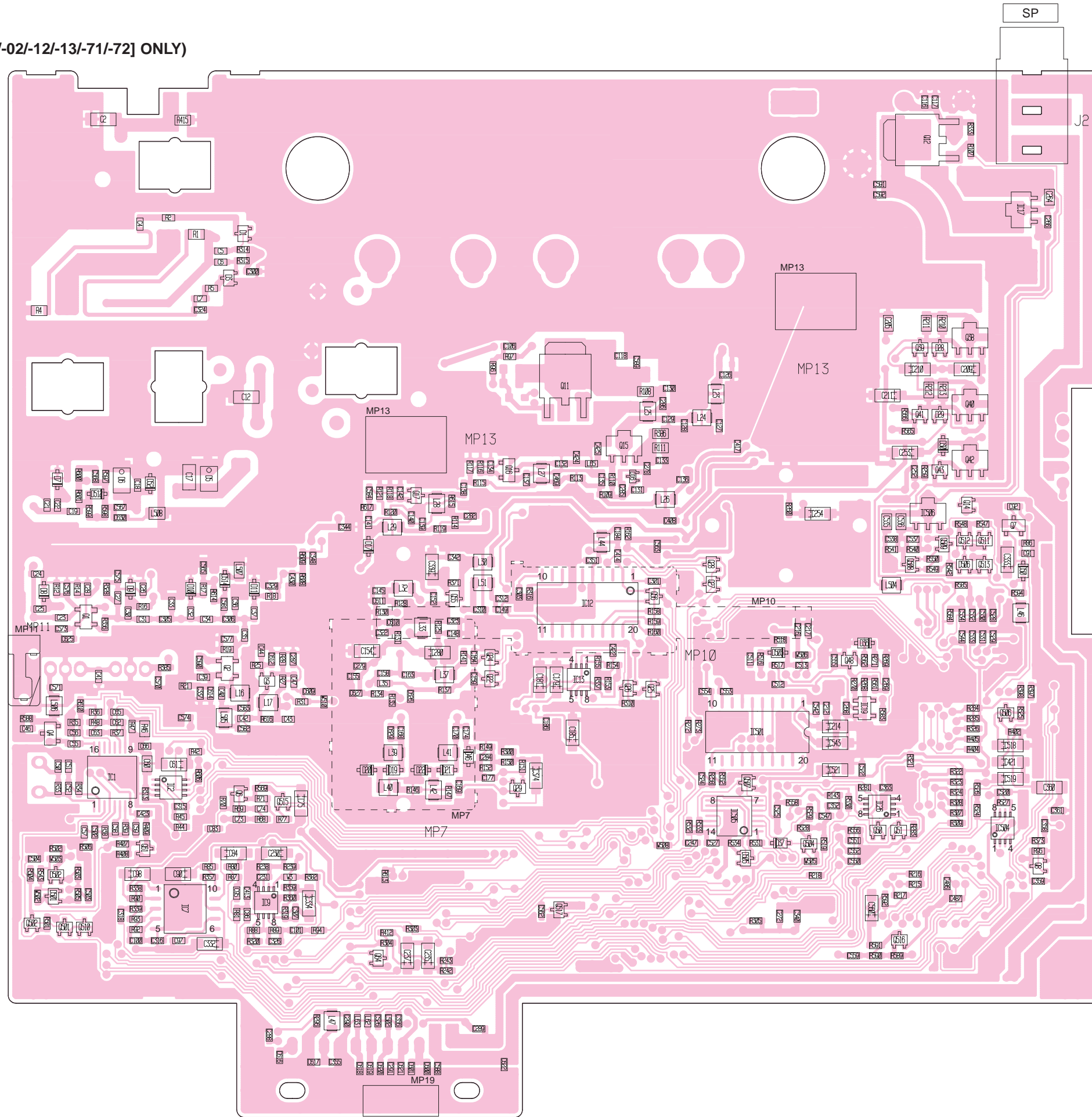
to optional unit
EX-1761 EEPROM

J5

1	VCC	12
	VCC	
	SP	
	SPE	
	+8V	
	FTXD	
	FRXD	
	POSW	
	MICE	
	MIC	
	GND	
	AFO	

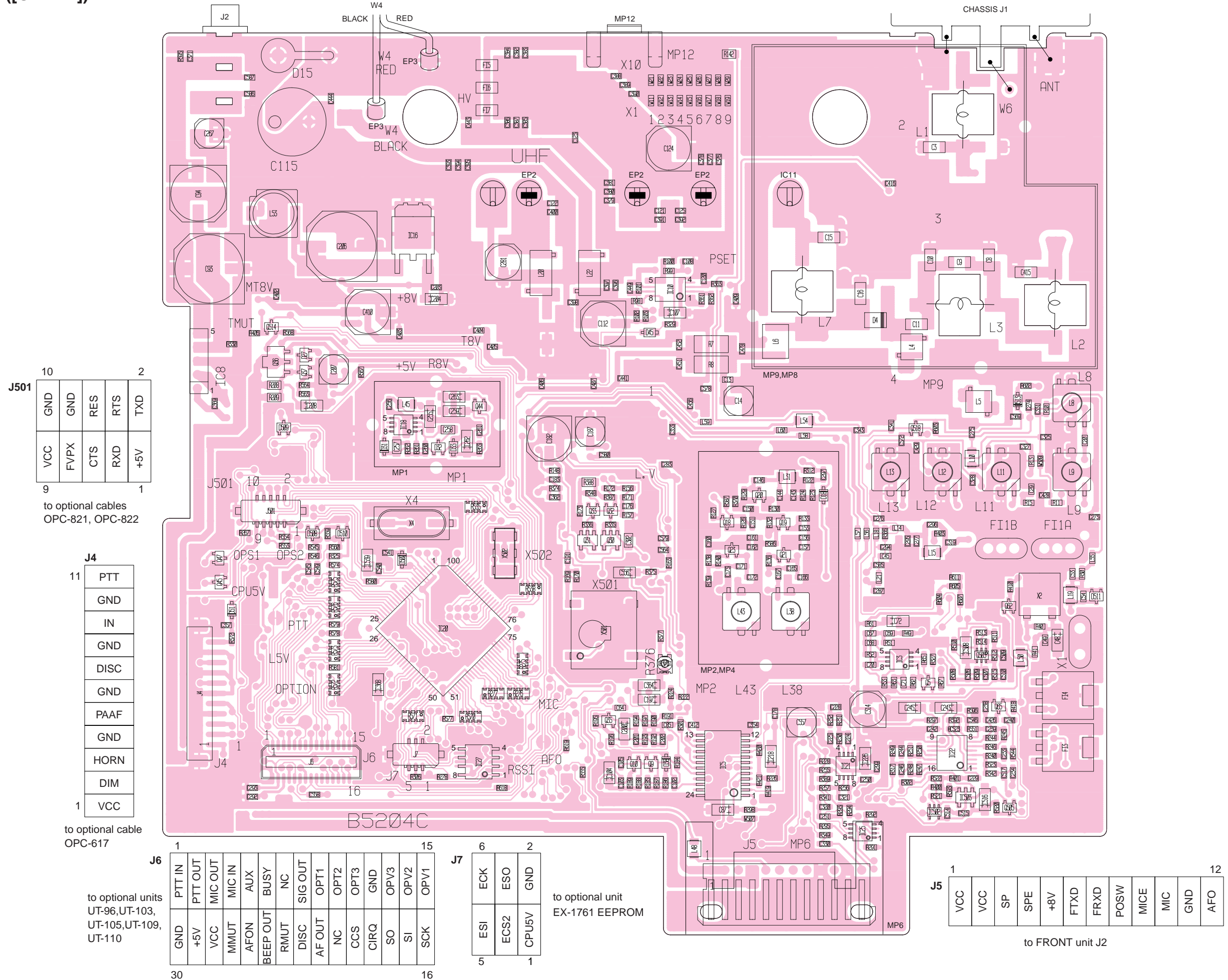
to FRONT unit J2

• BOTTOM VIEW (MAIN UNIT [EUR-01/02/12/13/71/72] ONLY)



9-3 MAIN UNIT ([OTHER])

• TOP VIEW



J501

10	GND	GND	RES	RTS	TXD
9	VCC	FVPX	CTS	RXD	+5V

to optional cables
OPC-821, OPC-822

J4

11	PTT
	GND
	IN
	GND
	DISC
	GND
	PAAF
	GND
	HORN
	DIM
1	VCC

to optional cable
OPC-617

to optional units
UT-96, UT-103,
UT-105, UT-109,
UT-110

J6

1	PTT IN	15	OPV1
2	PTT OUT	14	OPV2
3	MIC OUT	13	OPV3
4	MIC IN	12	GND
5	MIC IN	11	OPT3
6	AUX	10	OPT2
7	BUSY	9	OPT1
8	NC	8	SIG OUT
9	NC	7	DISC
10	RMUT	6	BEEP OUT
11	AFON	5	AFOUT
12	AFON	4	NC
13	AFON	3	CCS
14	AFON	2	CIRQ
15	AFON	1	SO

J7

6	ECK	2	GND
5	ECS2	1	ESU
4	ECS1		
3	ESU		
2	ESU		
1	ESU		

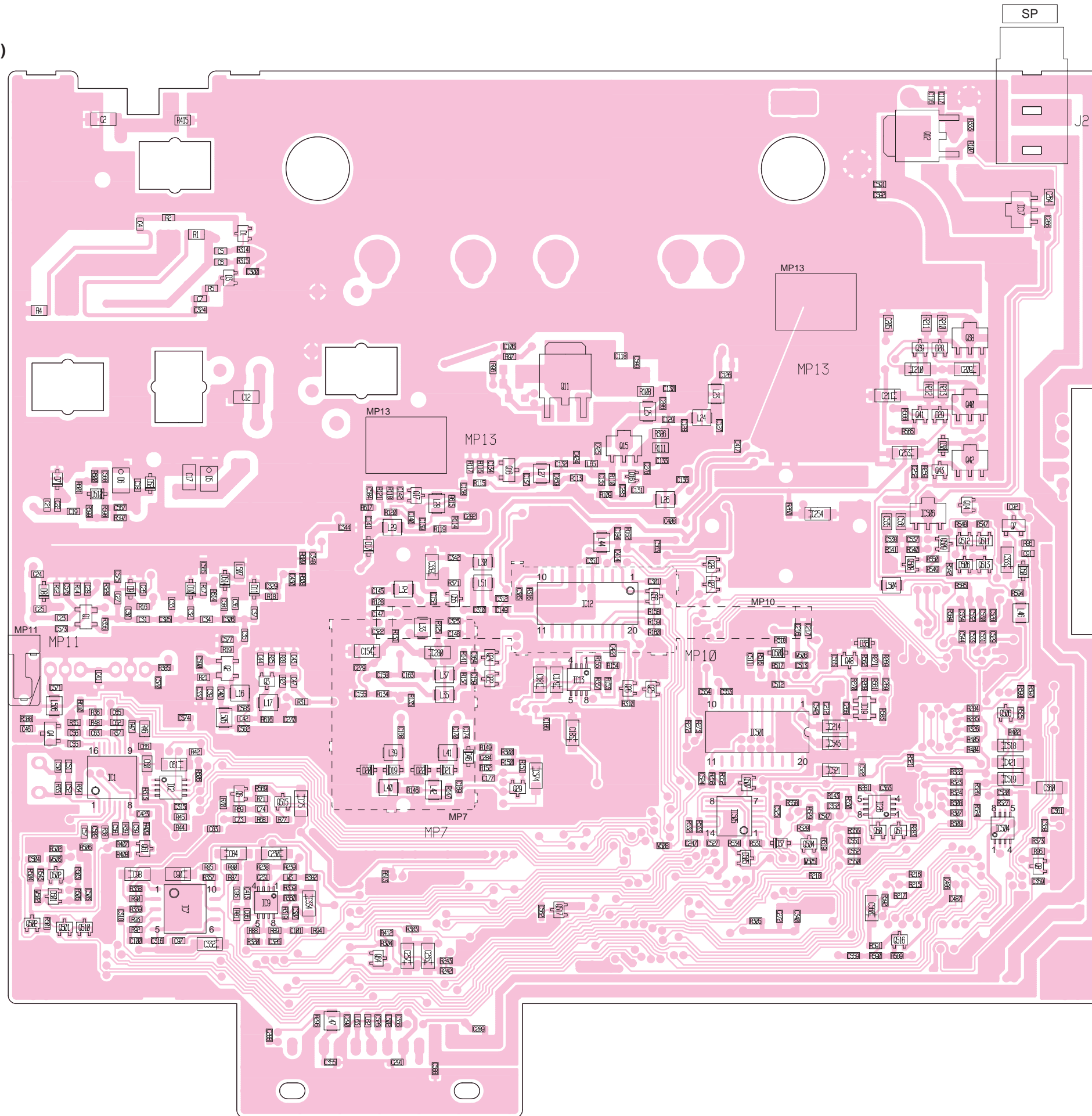
to optional unit
EX-1761 EEPROM

J5

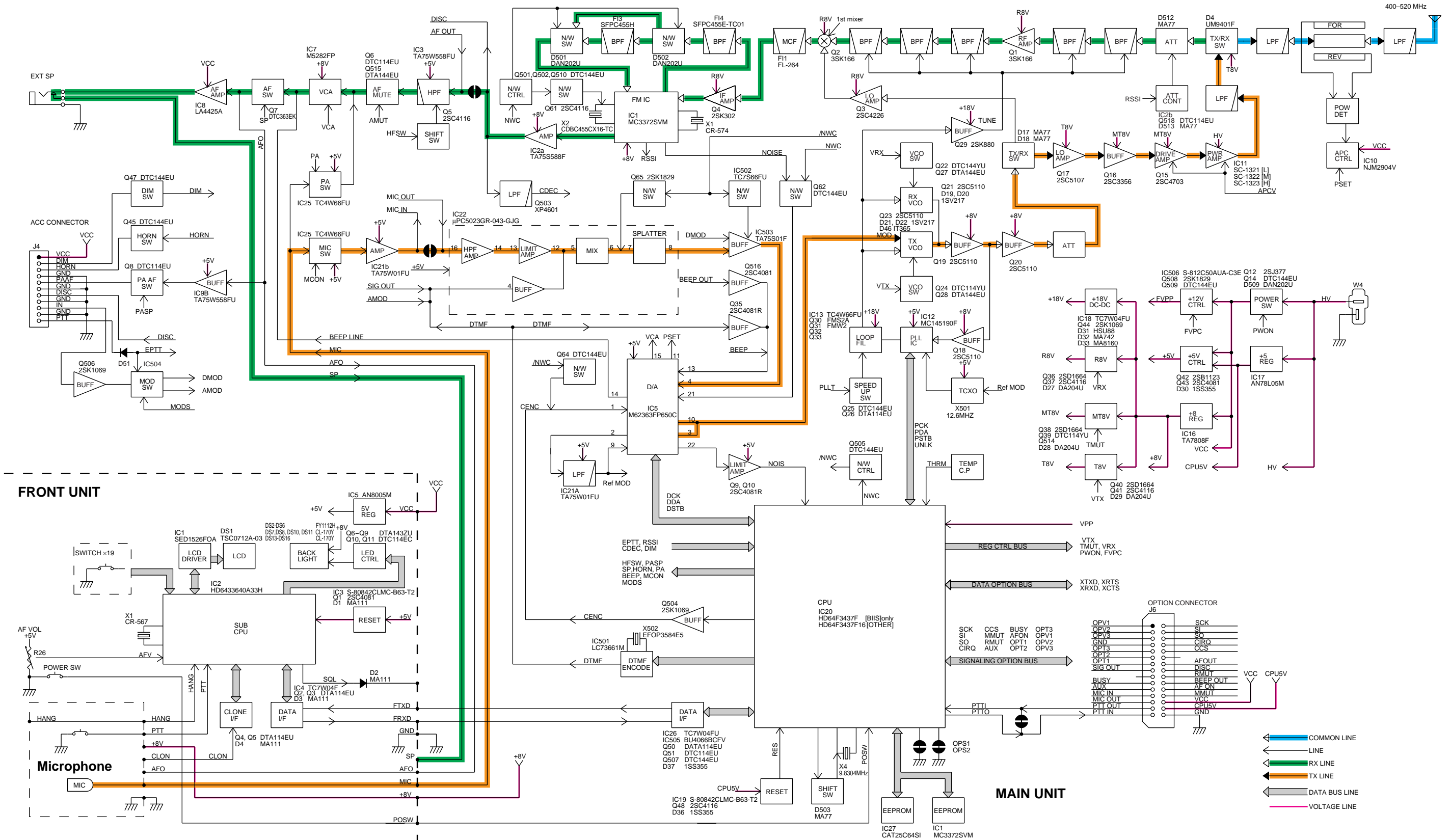
1	VCC	12	AFO
2	VCC	11	GND
3	SP	10	MIC
4	SPE	9	MICE
5	+8V	8	POSW
6	FTXD	7	FRXD
7	FRXD	6	FTXD
8	POSW	5	+8V
9	MICE	4	SPE
10	MIC	3	SP
11	GND	2	VCC
12	AFO	1	VCC

to FRONT unit J2

• BOTTOM VIEW (MAIN UNIT [OTHER])

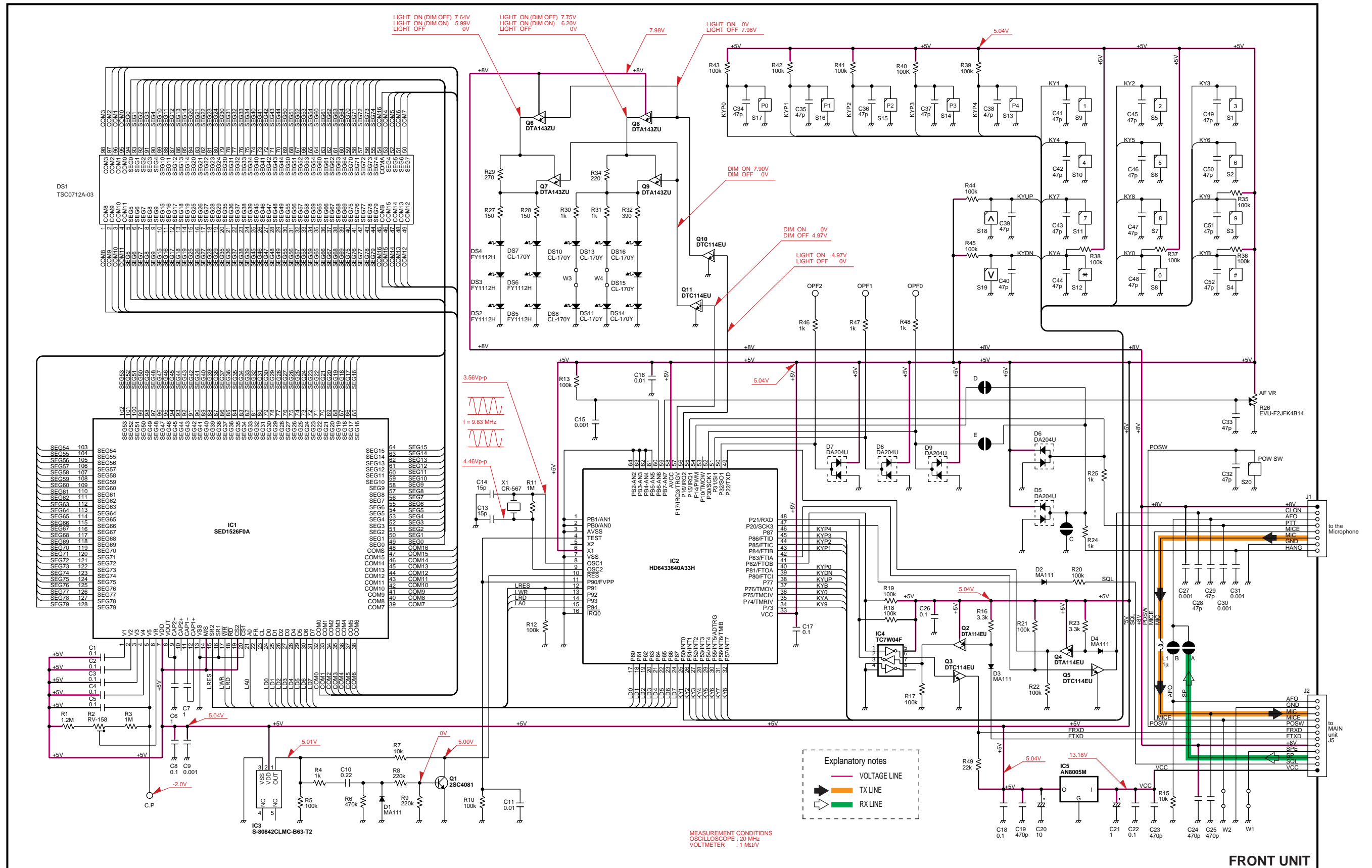


SECTION 10 BLOCK DIAGRAM

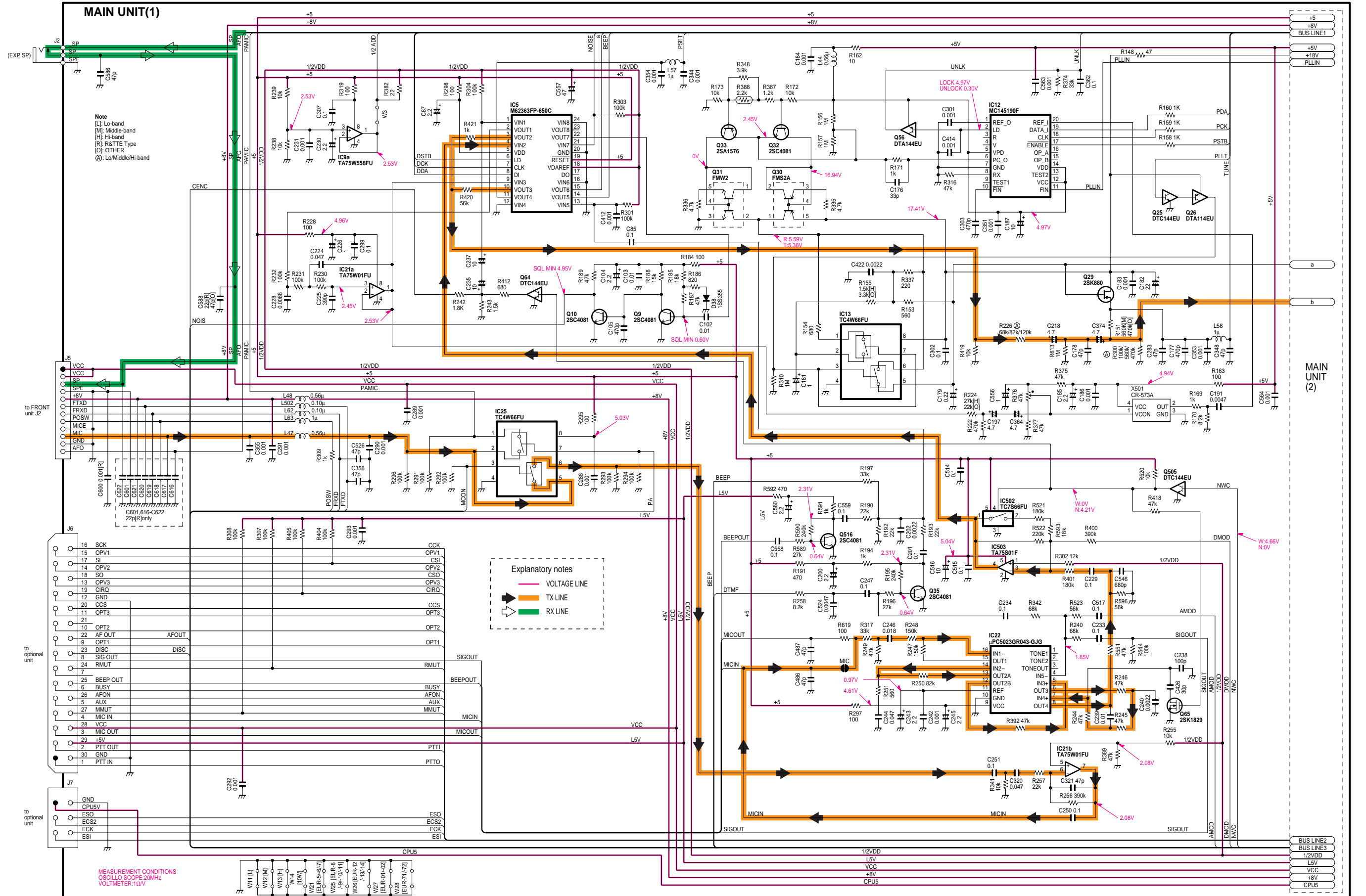


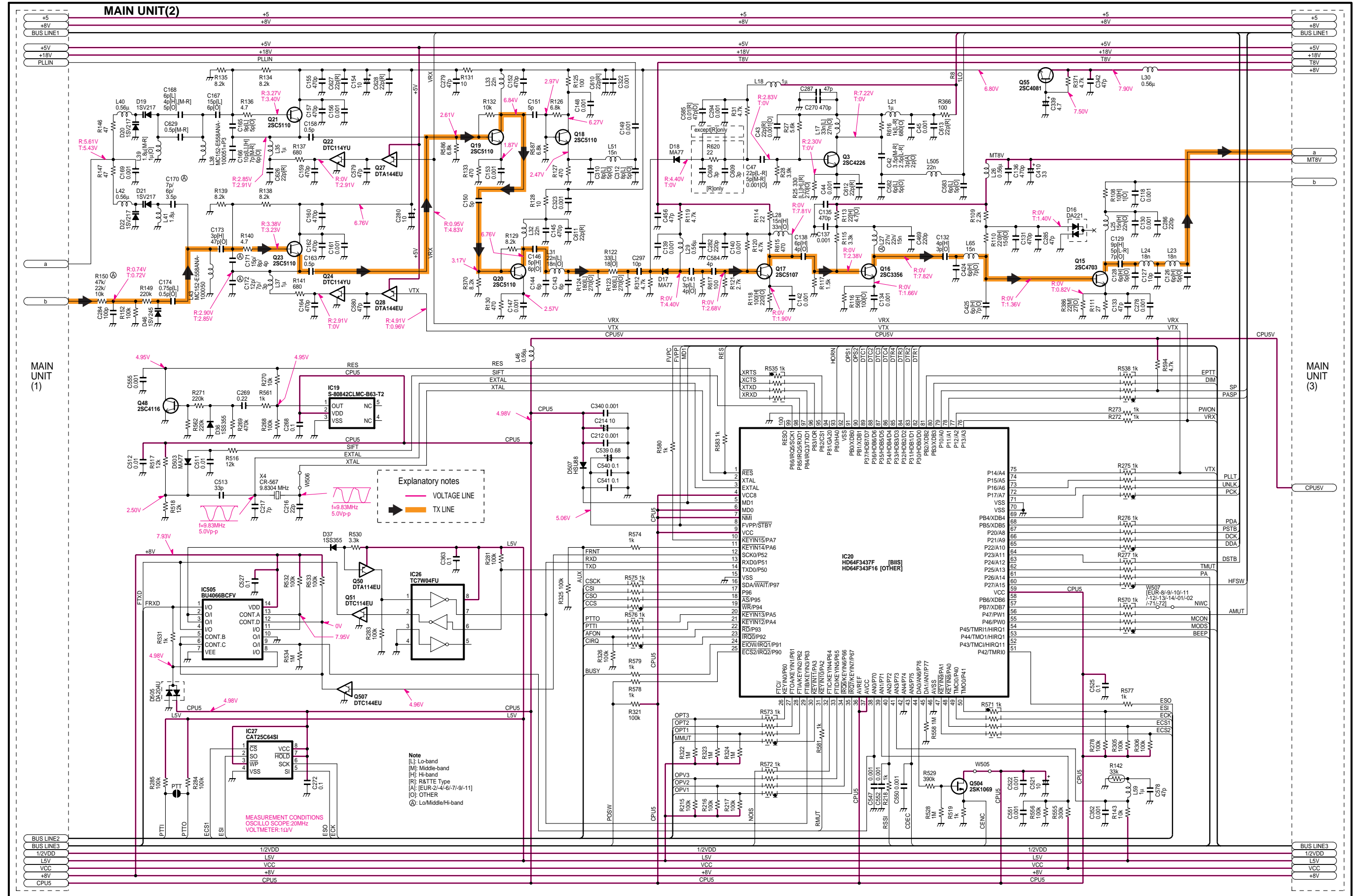
SECTION 11 VOLTAGE DIAGRAMS

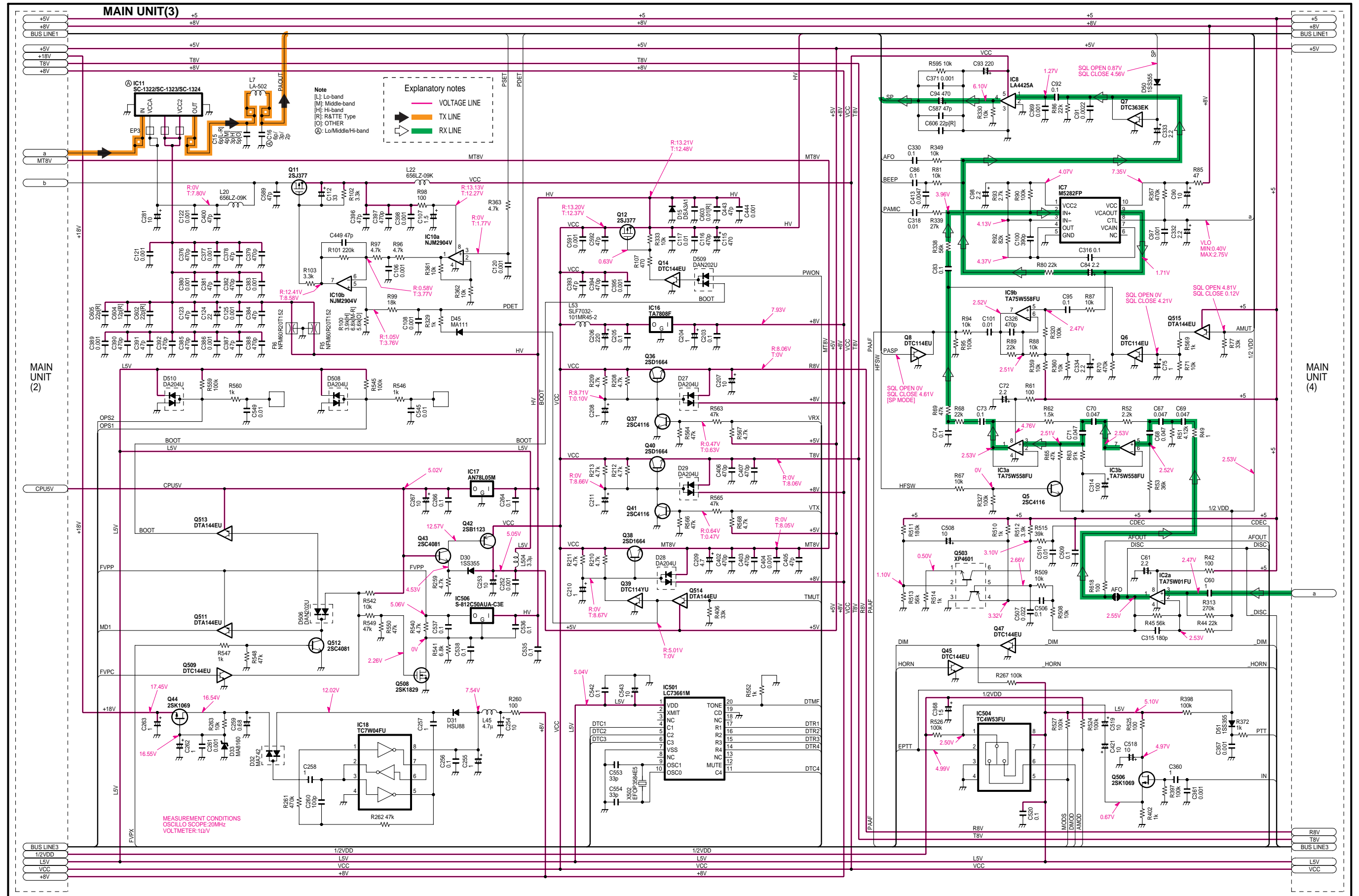
11-1 FRONT UNIT

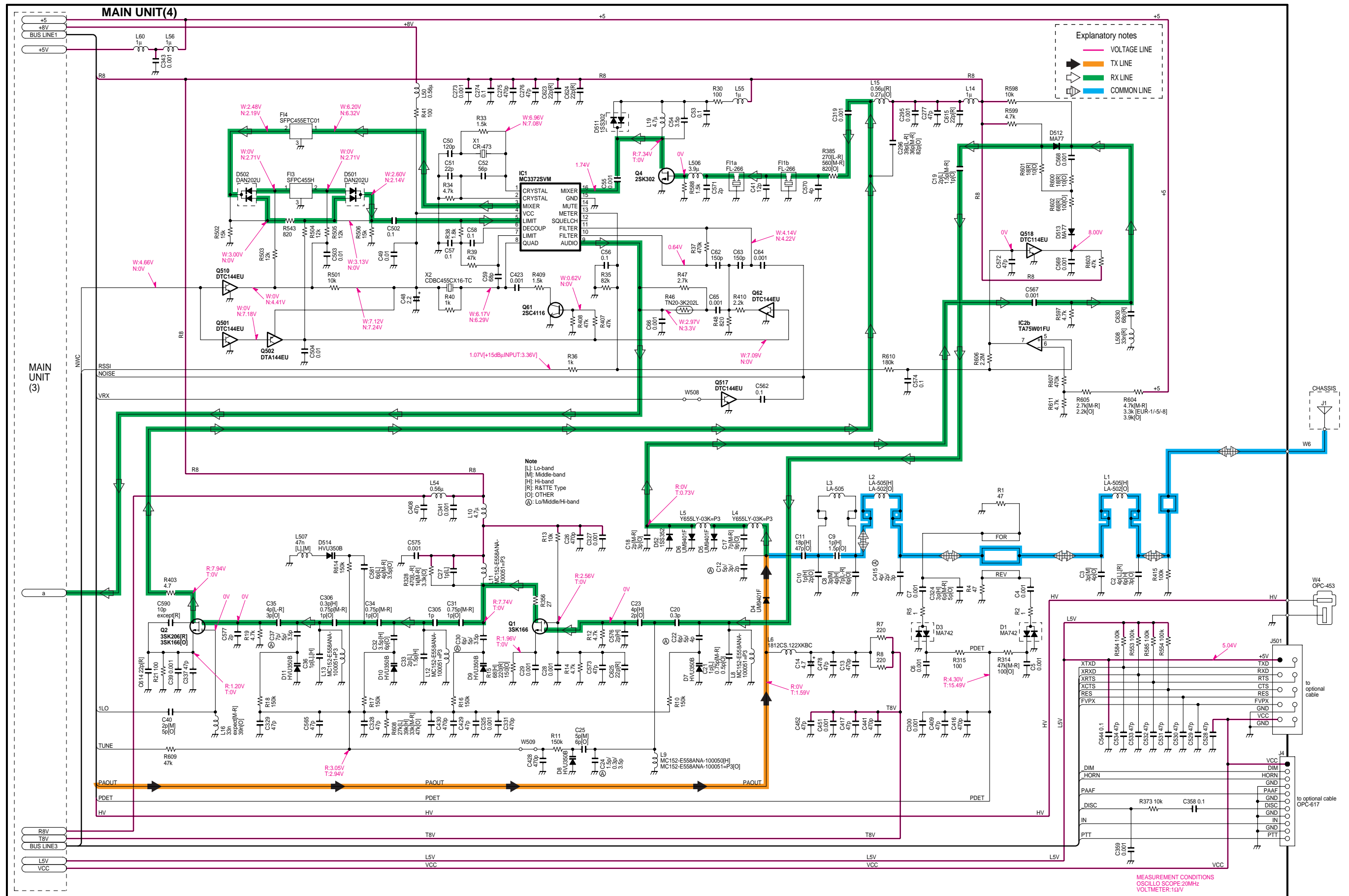


11-2 MAIN UNIT



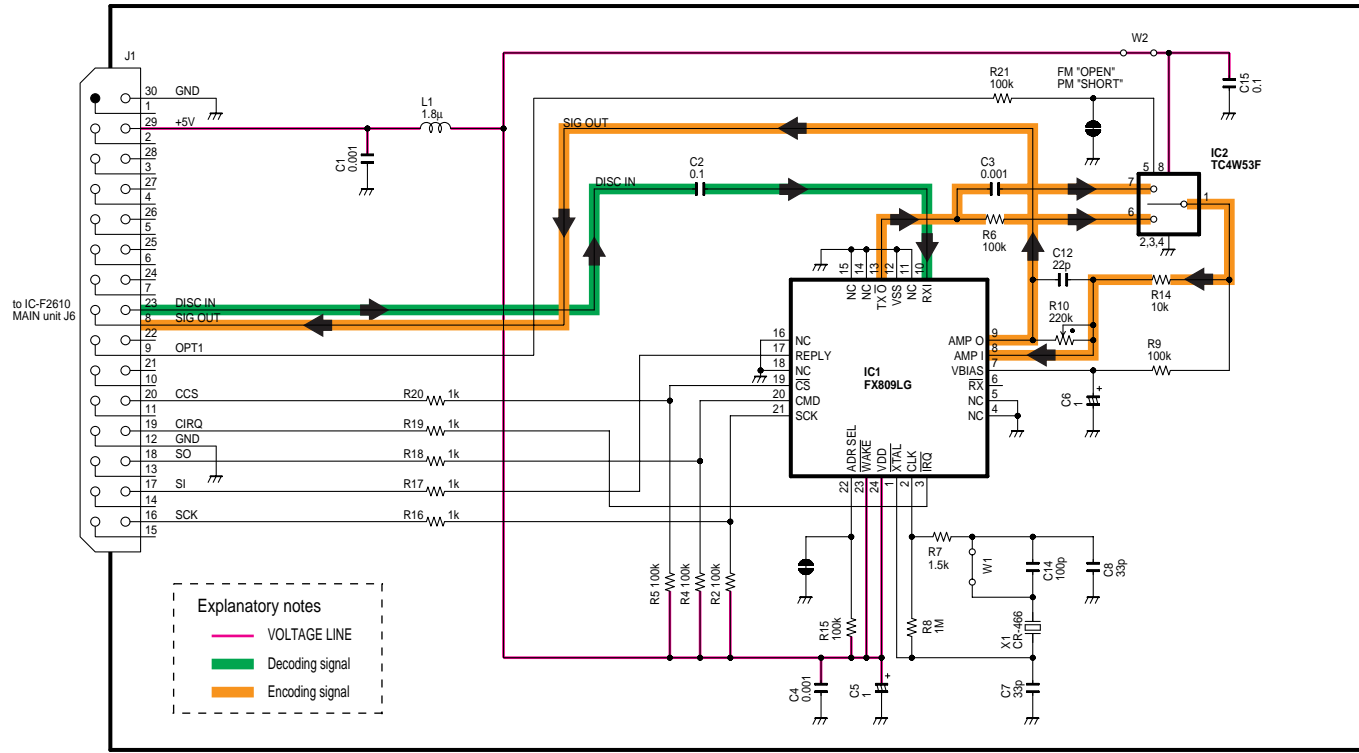




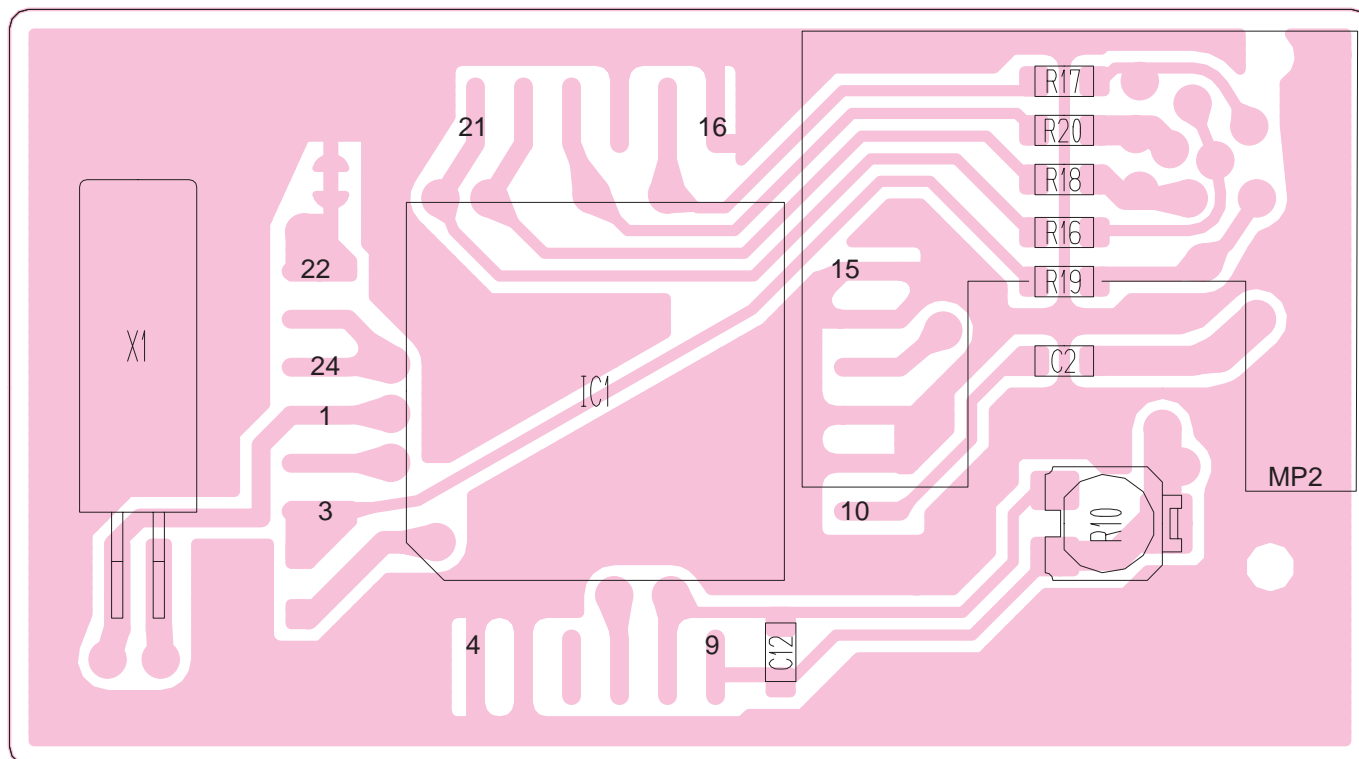


SECTION 12 OPTIONAL UNIT UT-103

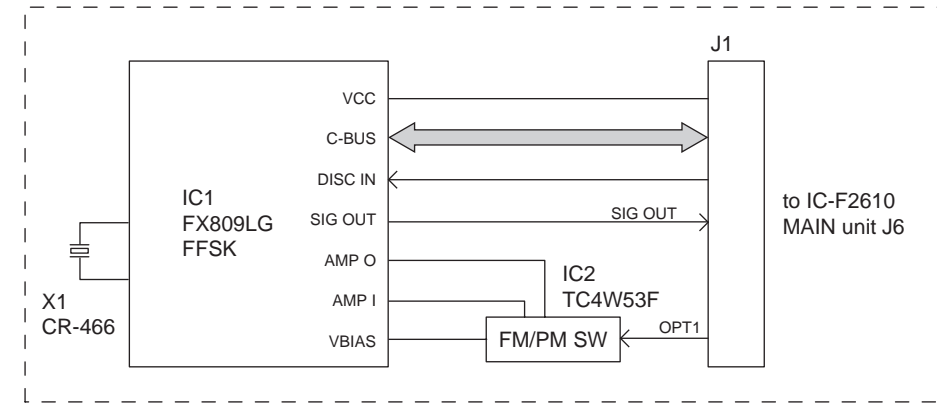
• SCHEMATIC DIAGRAM



• BOARD LAOUT (TOP VEIW)



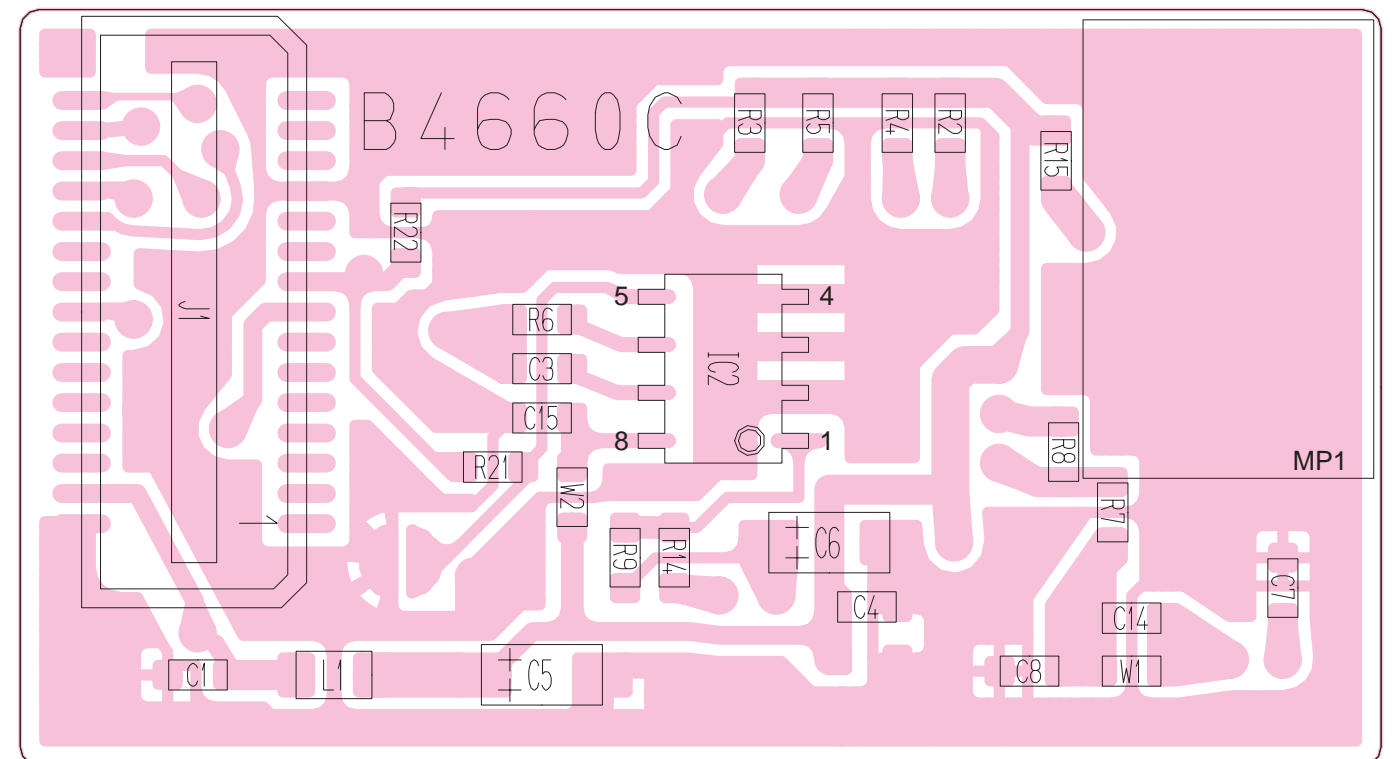
• BLOCK DIAGRAM



• BOARD LAYOUT (BOTTOM VIEW)

16	SCK	NC	15
	SI	NC	
	SO	NC	
	CIRQ	GND	
	CCS	NC	
	NC	NC	
	NC	OPT1	
	DISC IN	SIG OUT	
	NC	NC	
	NC	NC	
	NC	NC	
	NC	NC	
	NC	NC	
	+5V	NC	
30	GND	NC	1

to IC-F2610
MAIN unit J6



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Fax : +81 (06) 6793 0013
URL : <http://www.icom.co.jp/world/index.html>

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